

**FH3210GS****N-Channel SGT Power MOSFET****◆ General Description**

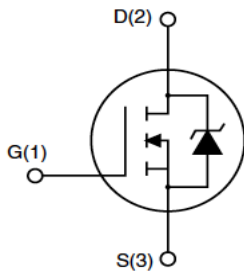
This N channel SGT MOSFET has been designed to very low on-state resistance and superior E_{AS} performance, especially for BMS and Motor driving applications.

◆ Features

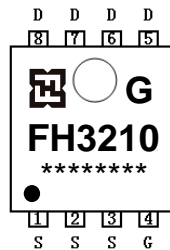
- $R_{DS(ON)} = 4.5 \text{ m}\Omega$ (Typ) @ $V_{GS}=10\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

◆ Applications

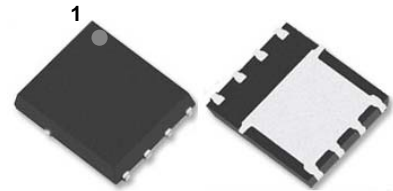
- Power Management
- DC/DC Converter
- Load Switch



Schematic diagram



Marking and pin Assignment



PDFN5x6-8L top and bottom view

Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	100	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) (Note 1)	78	A
	Drain Current - Continuous ($T_C = 100^\circ\text{C}$)	64	A
I_{DM}	Drain Current - Pulsed (Note 2)	312	A
V_{GS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 3)	225	mJ
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	76	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Steady-State	3.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Steady State (Note 4)	63.7	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V},$			1	μA
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(TH)}$	Gate Threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2	3	4	V
$R_{DS(ON)}$	Drain-Source on-state resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		4.5	5.4	m Ω
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$ $F = 1\text{ MHz}$		3244		pF
C_{OSS}	Output Capacitance			1077		pF
C_{RSS}	Reverse Transfer Capacitance			52		pF
R_G	Gate Resistance	$F = 1\text{ MHz}$		3.5		Ω
Switching Characteristics						
$T_{D(ON)}$	Turn On Delay Time	$V_{DD} = 50\text{ V}, R_L = 2.5\ \Omega,$ $V_{GS} = 10\text{ V}, R_G = 6\ \Omega$		22		nS
T_R	Rise Time			36		nS
$T_{D(OFF)}$	Turn Off Delay Time			49		nS
T_F	Fall Time			31.5		nS
Q_G	Total Gate Charge	$V_{DD} = 50\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}$		51.3		nC
Q_{GS}	Gate-Source Charge			15.2		nC
Q_{GD}	Gate-Drain Charge			13.1		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Body-Diode Forward Current				78	A
I_{SM}	Maximum Pulsed Body-Diode Forward Current ^(NOTE 1)				312	A
V_{SD}	Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1\text{ A}$		0.7	1	V
T_{RR}	Reverse recovery time	$V_{DD} = 50\text{ V}, I_D = 15\text{ A},$ $di/dt = 100\text{ A}/\mu\text{S}$		58		ns
Q_{RR}	Reverse recovery charge			90.0		nC
I_{RRM}	Peak Reverse Recovery Current			2.6		A

Notes:

1. The max drain current rating is package limited
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. $L = 0.5\text{ mH}, V_{DD} = 50\text{ V}, I_{AS} = 30\text{ A}, R_G = 25\ \Omega,$ Starting $T_J = 25^\circ\text{C}$
4. Mount on minimum PCB layout

Electrical Characteristics Diagrams

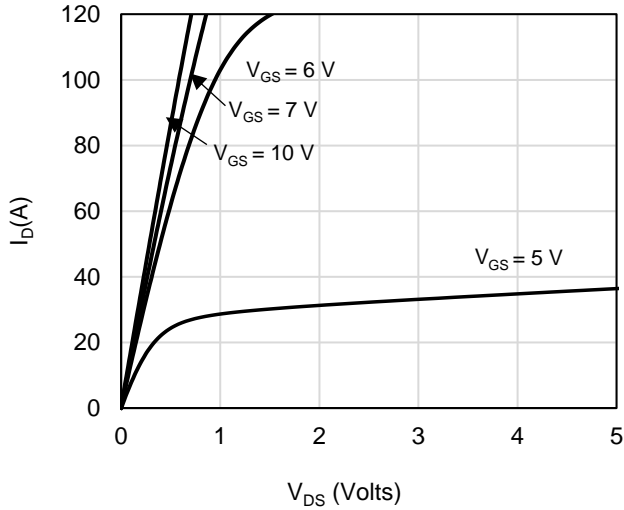


Figure 1: On-Region Characteristics

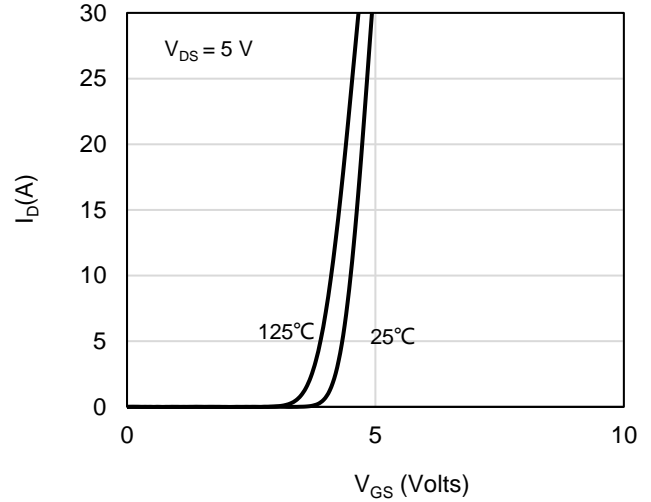


Figure 2: Transfer Characteristics

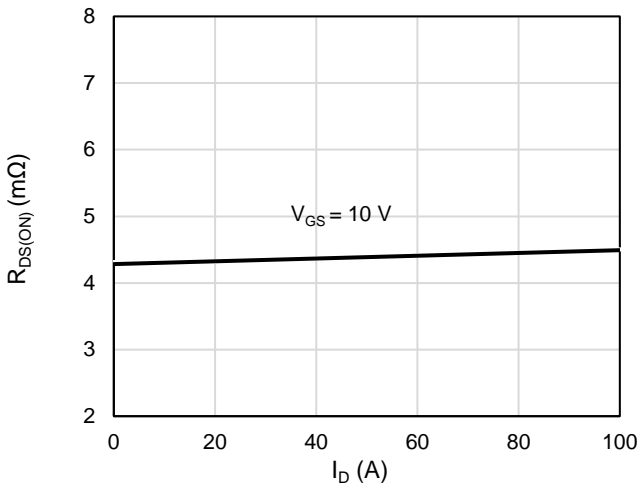


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

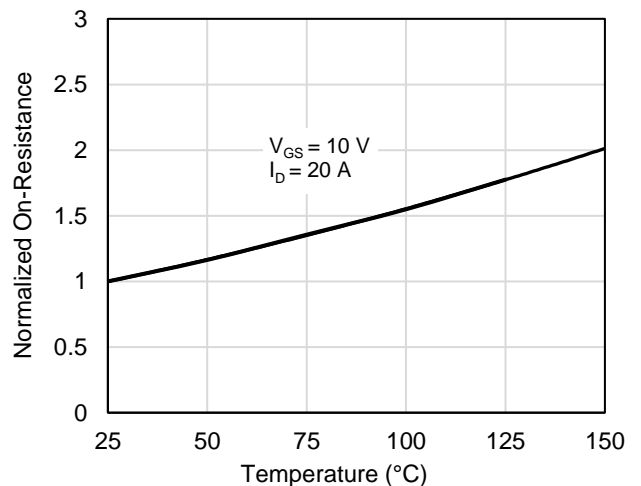


Figure 4: On-Resistance vs. Junction Temperature

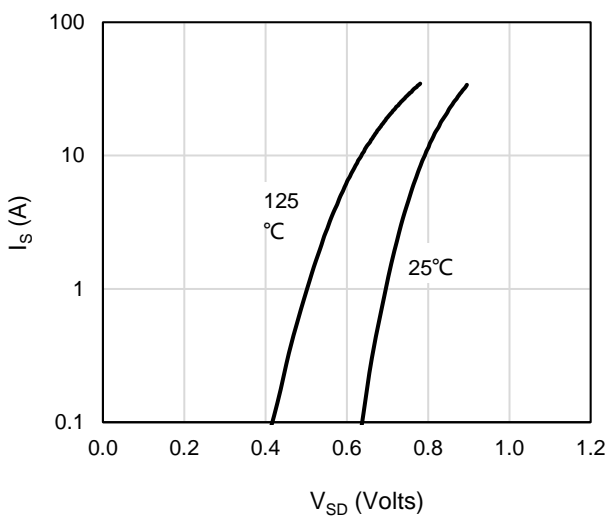


Figure 7: Body-Diode Characteristics

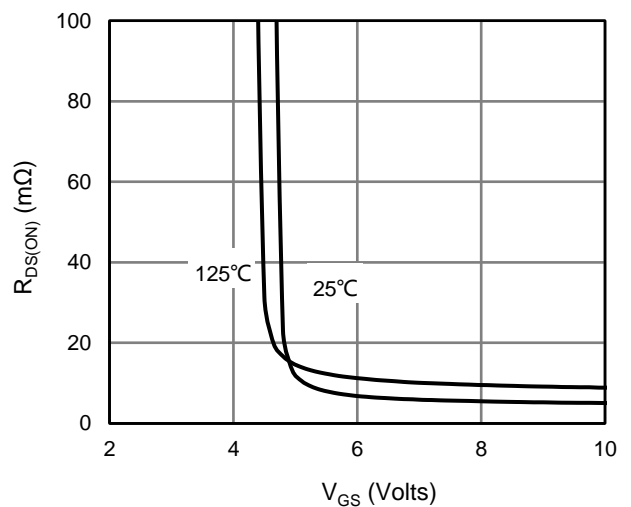


Figure 8: On-Resistance vs. Gate-Source Voltage

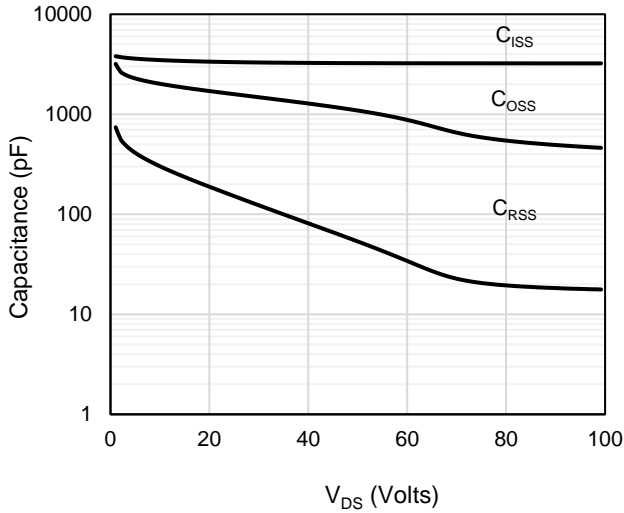


Figure 9: Capacitance Characteristics

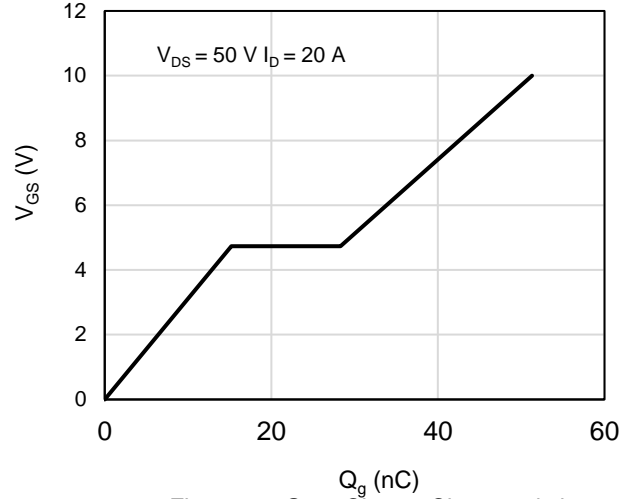


Figure 10: Gate-Charge Characteristics

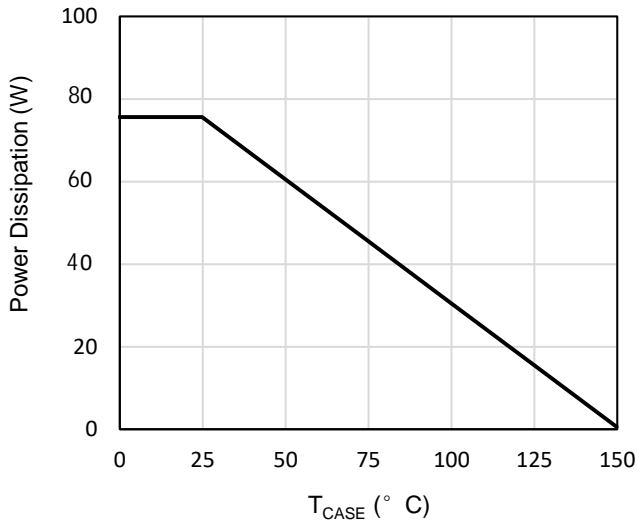


Figure 11: Power De-rating

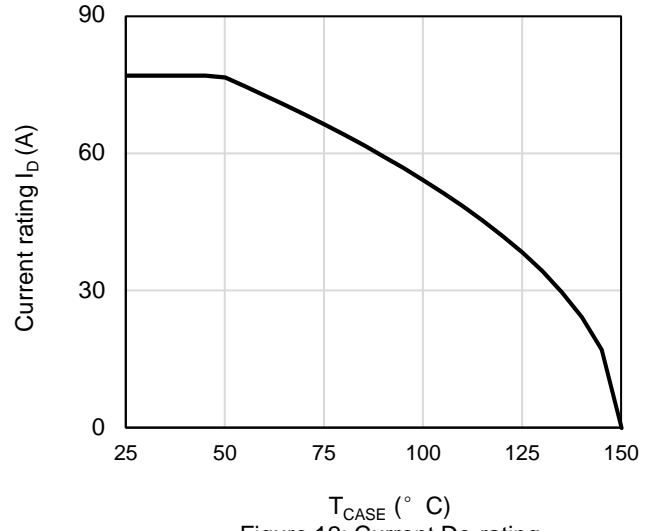


Figure 12: Current De-rating

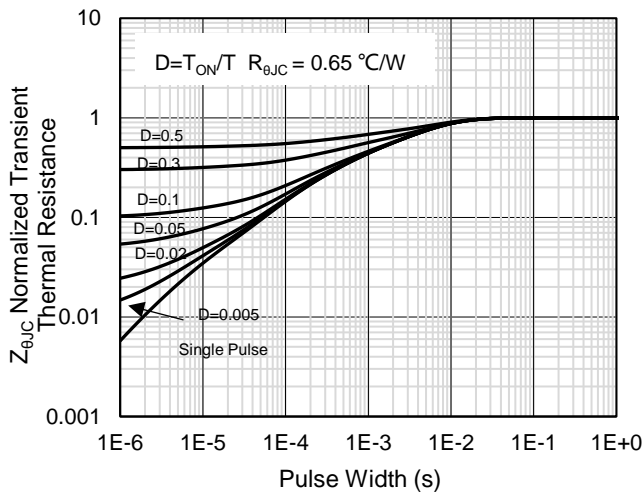


Figure 13: Normalized Maximum Transient Thermal Impedance

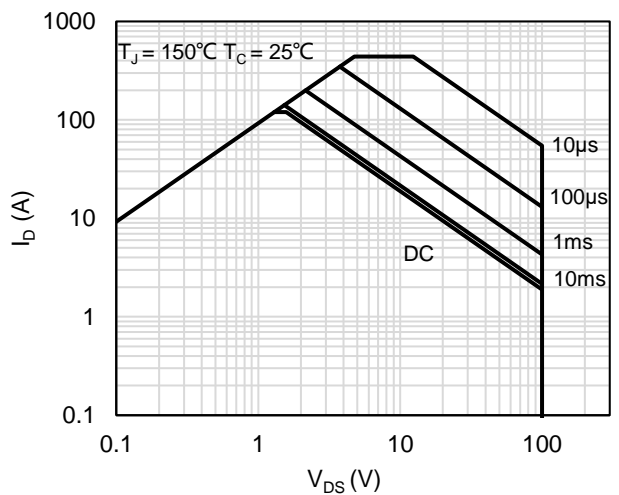
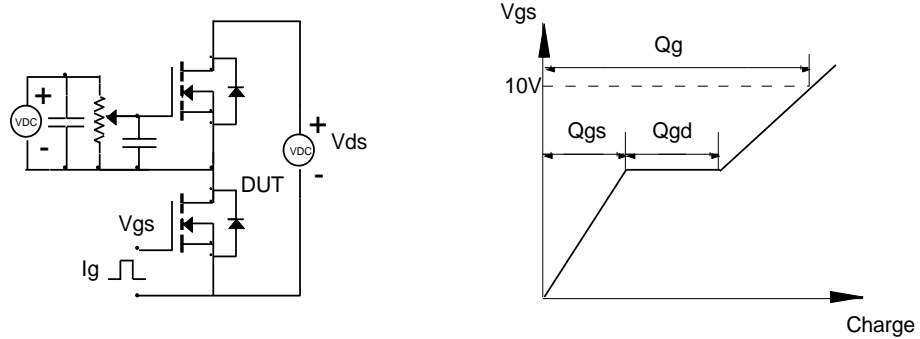


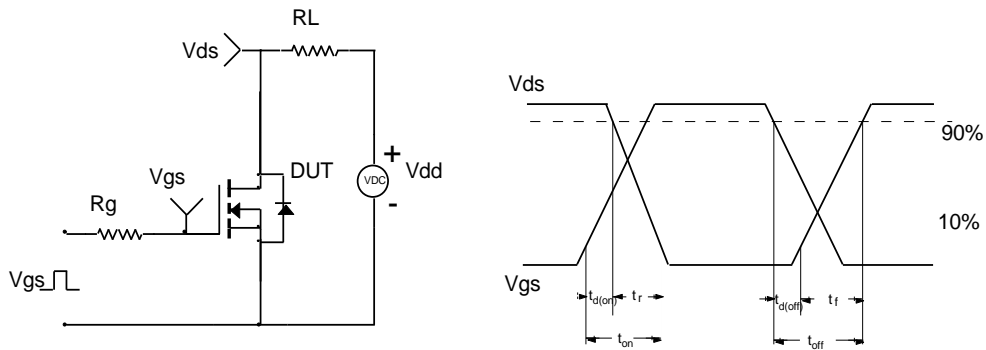
Figure 14: Maximum Forward Biased Safe Operating Area

Test Circuit and Waveform

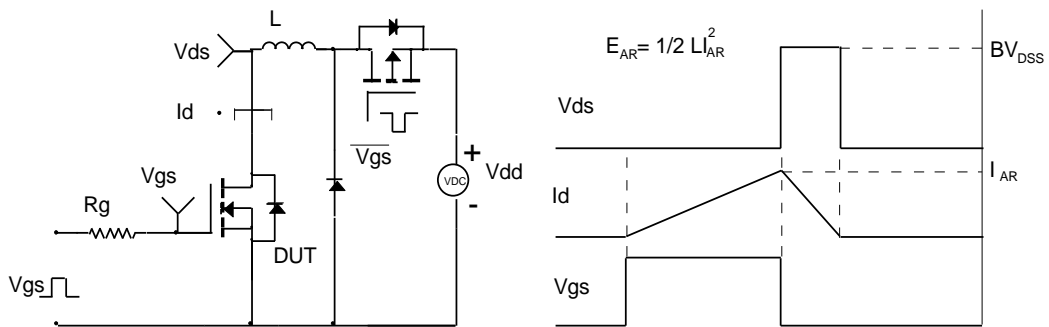
Gate Charge Test Circuit & Waveform



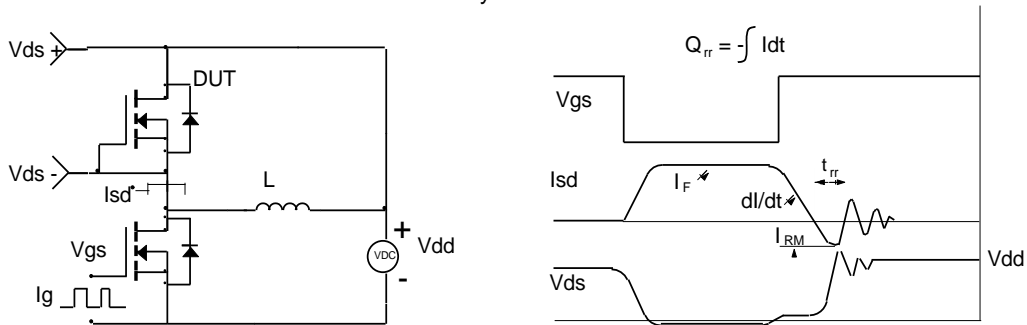
Resistive Switching Test Circuit & Waveforms



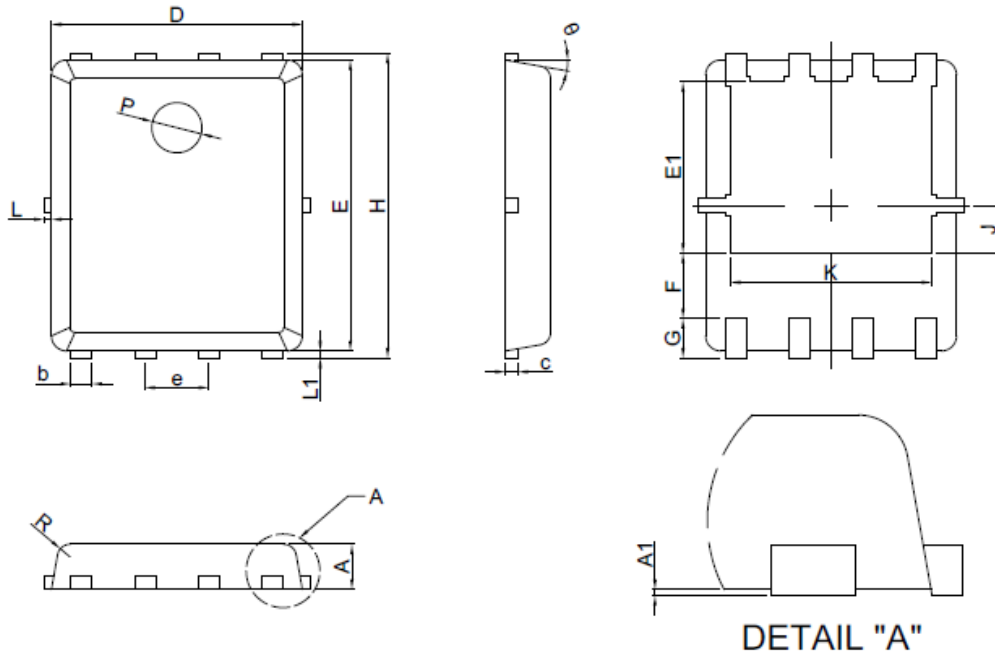
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Information : PDFN5x6-8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	0.80	1.00
A1	0.00	0.05
b	0.35	0.49
c	0.254REF	
D	4.80	5.20
F	1.40REF	
E	5.60	5.90
e	1.27BSC	
H	5.80	6.20
L1	0.10	0.18
G	0.60REF	
K	4.00REF	
L	-	0.15
J	0.95BSC	
P	1.00REF	
E1	3.40REF	
θ	6°	14°
R	0.25REF	