FH4504TL

N-Channel Trench Power MOSFET

◆ General Description

The FH4504TL is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

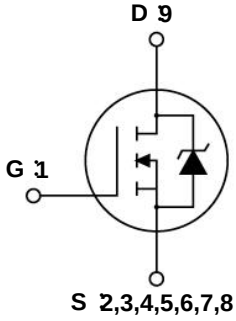
◆ Applications

- High power inverter system
- LCD TV appliances
- Load Switch

◆ Features

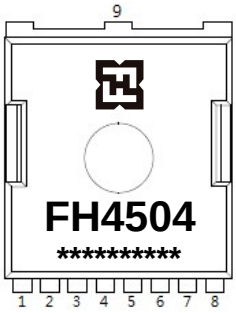
Parameter	Typ.	Unit
V_{DS}	40	V
I_D (@ V_{GS} = 10V)	250	A
$R_{DS(ON)}$ (@ V_{GS} = 10V) (Typ)	1.2	mΩ
$R_{DS(ON)}$ (@ V_{GS} = 4.5V) (Typ)	1.9	mΩ

- Surface-mounted package
- Advanced trench cell design
- Super Trench



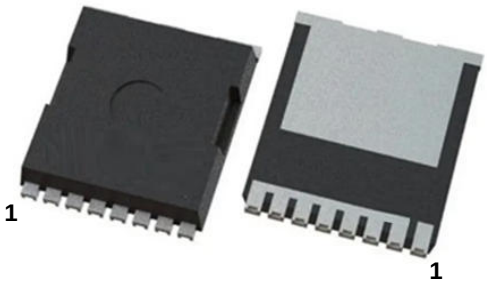
Schematic diagram

Top view



Marking and pin assignment

TOLL-8L



Top view Bottom View

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C = 25 ℃	40	-	V
V_{GS}	Gate-Source Voltage	T_C = 25 ℃	-	±20	V
I_D* ***	Drain Current (DC)	T_C = 25 ℃, V_{GS} = 10 V	-	250	A
I_{DM}**,***	Drain Current (Pulsed)	T_C = 25 ℃, V_{GS} = 10 V	-	1300	A
P_{tot}	Drain power dissipation	T_C = 25 ℃	-	300	W
T_{stg}	Storage Temperature		-55	150	℃
T_J	Junction Temperature		-	150	℃
I_S	Continuous-Source Current	T_C = 25 ℃	-	250	A
E_{AS}	Single Pulsed Avalanche Energy	V_{DD}=40V , L=1.0mH	-	1052	mJ
$R_{\theta JA}$**	Thermal Resistance- Junction to Ambient		-	40	℃/W
$R_{\theta JC}$**	Thermal Resistance- Junction to Case		-	0.5	

Notes：

* Surface Mounted on minimum footprint pad area.

** Pulse width ≤ 300 μs, duty cycle ≤ 2 %

*** Maximum current rating is package limited.

Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

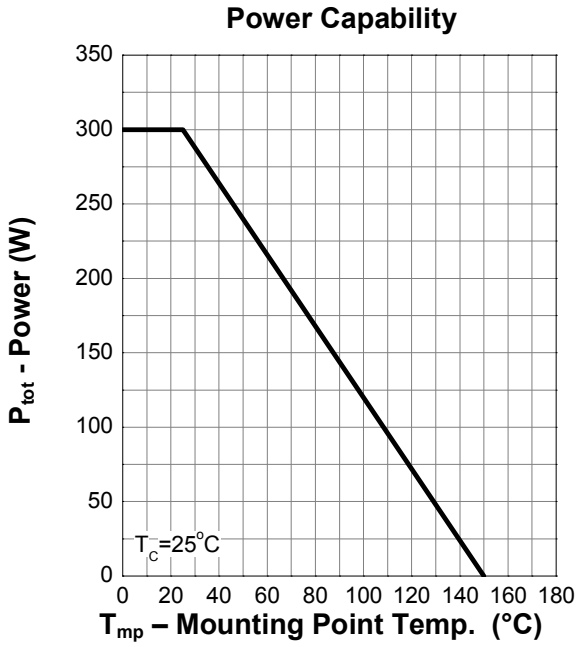
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	40	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.5	2.0	2.5	V
I_{DSS}	Zero Gate Voltage Source Current	V_{DS} = 32 V, V_{GS} = 0 V	-	-	1	µA
		T_J = 85 ℃	-	-	30	µA
I_{GSS}	Gate Leakage Current	V_{GS} = ± 20 V, V_{DS} = 0 V	-	-	± 100	nA
$R_{DS(ON)}$ [a]	Drain-Source On-State Resistance	V_{GS} = 10 V, I_D = 20 A	-	1.2	1.5	mΩ
		V_{GS} = 4.5 V, I_D = 10 A	-	1.9	2.5	
Diode Characteristics						
V_{SD} [a]	Diode Forward Voltage	I_{SD} = 20 A, V_{GS} = 0 V	-	-	1.3	V
t_{rr}	Reverse Recovery Time	I_{SD} = 20 A, dI_{SD}/dt = 100 A/µs	-	68	-	ns
Q_{rr}	Reverse Recovery Charge		-	92	-	nC
Dynamic Characteristics [b]						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 20 V Frequency = 1 MHz	-	4925	-	pF
C_{oss}	Output Capacitance		-	1655	-	
C_{rss}	Reverse Transfer Capacitance		-	122	-	
t_d(on)	Turn-on Delay Time	V_{DS} = 20 V, V_{GEN} = 10 V, R_G = 4.5 Ω, R_L = 1 Ω, I_{DS} = 20 A	-	16	-	ns
t_r	Turn-on Rise Time		-	48	-	
t_d(off)	Turn-off Delay Time		-	75	-	
t_f	Turn-off Fall Time		-	42	-	
Gate Charge Characteristics [b]						
Q_g	Total Gate Charge	V_{DS} = 20 V, V_{GS} = 10 V, I_{DS} = 20 A	-	81	-	nC
Q_{gs}	Gate-Source Charge		-	18	-	
Q_{gd}	Gate-Drain Charge		-	15	-	

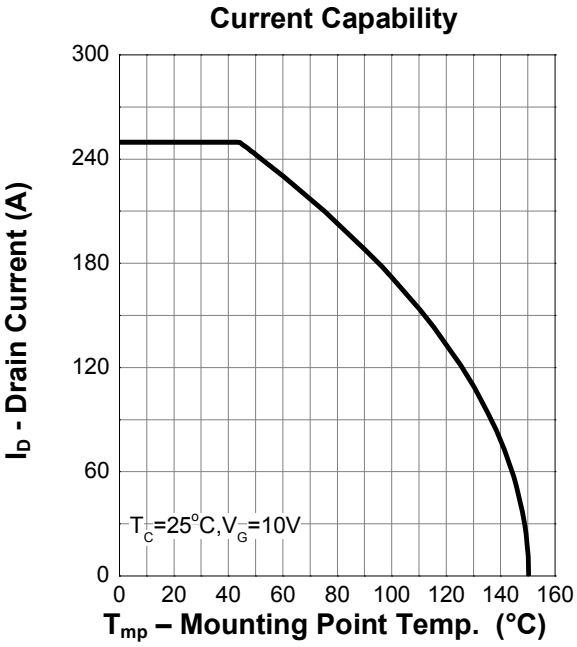
Notes :

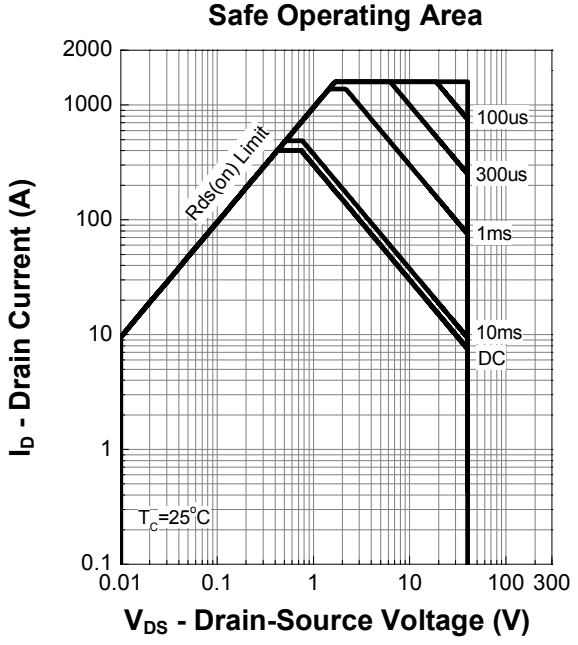
a : Pulse test ; pulse width ≤ 300 µs, duty cycle ≤ 2 %

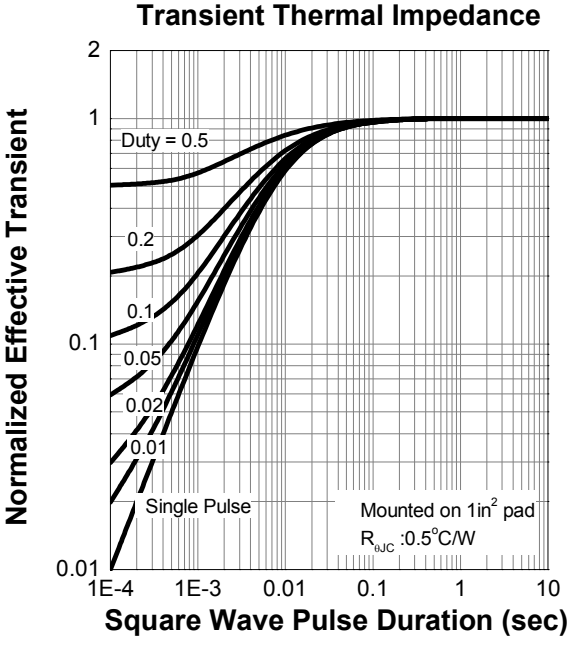
b : Guaranteed by design, not subject to production testing

Typical Characteristics



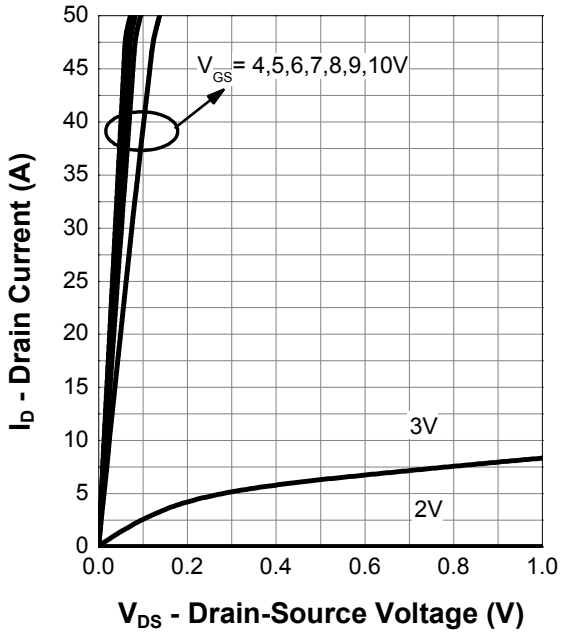




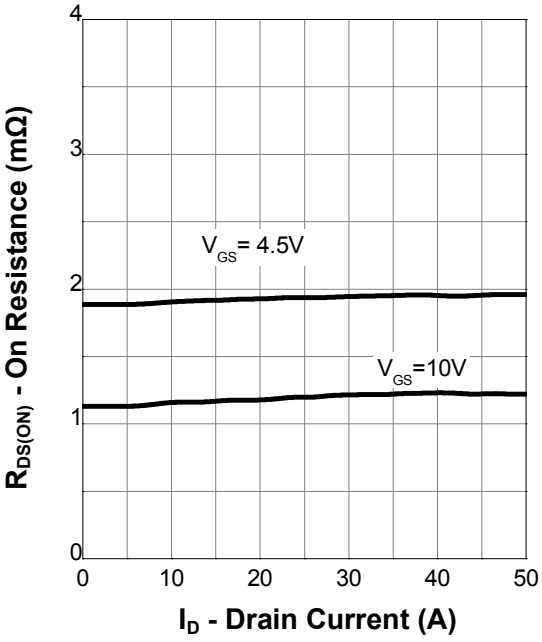


Typical Characteristics (Cont.)

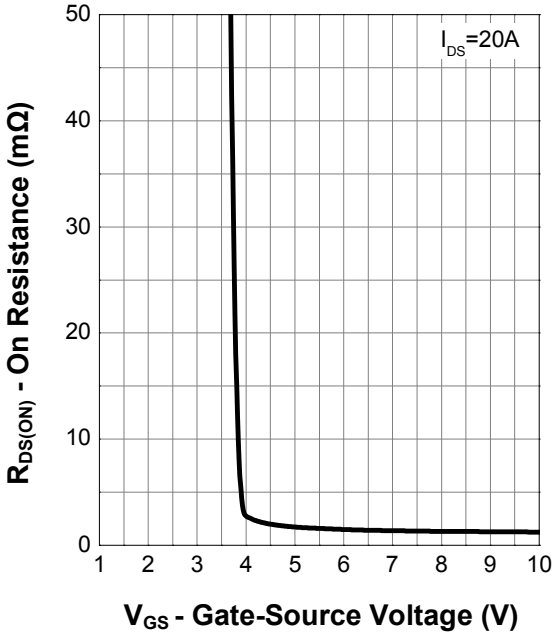
Output Characteristics



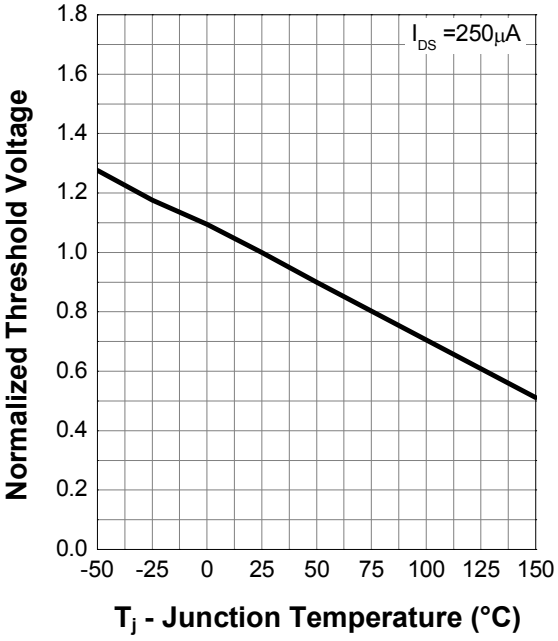
On Resistance



Transfer Characteristics

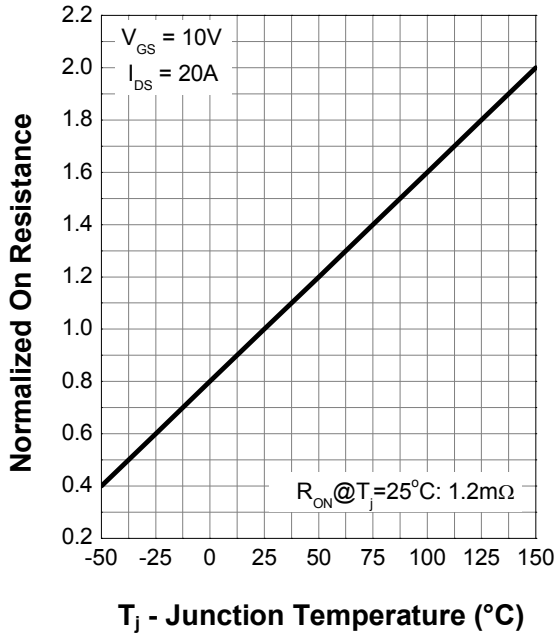


Normalized Threshold Voltage

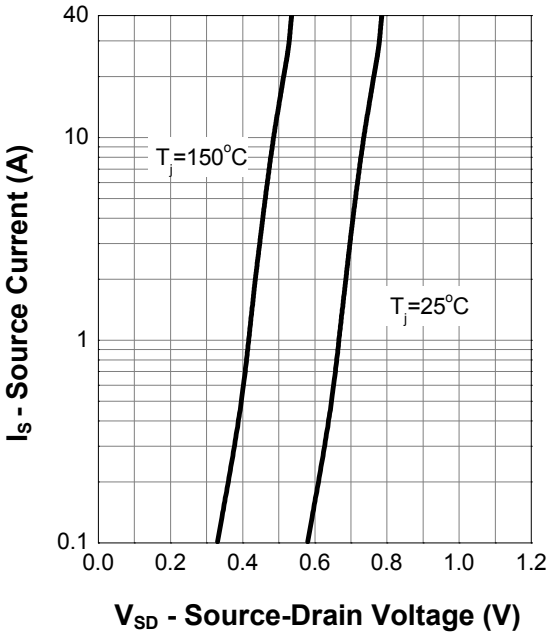


Typical Characteristics (Cont.)

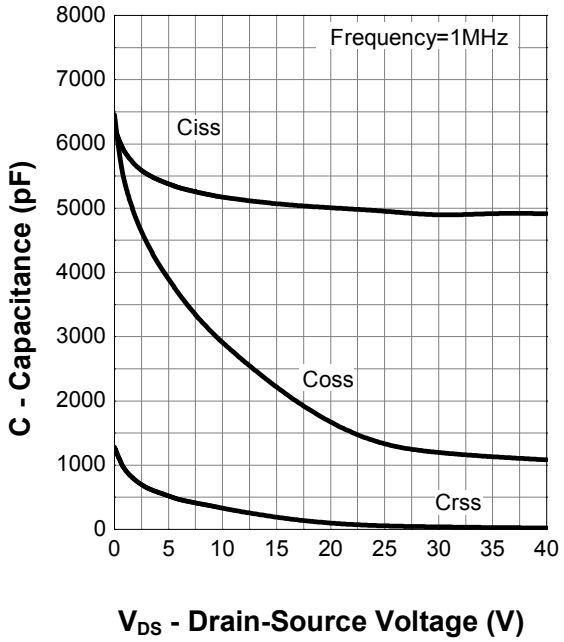
Normalized On Resistance



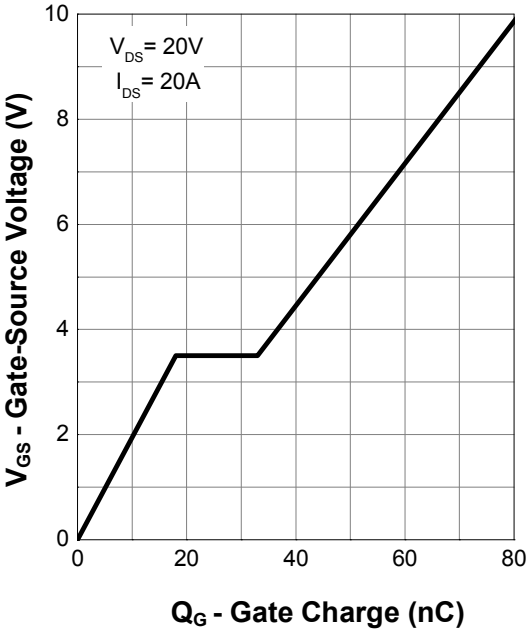
Diode Forward Current



Capacitance



Gate Charge



Package Information ：TOLL-8L