

Description

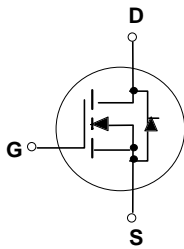
The FH1908D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

General Features

- $V_{DS} = 80V, I_D = 80A$
 $R_{DS(ON)} < 7.9m\Omega @ V_{GS}=10V$ (Typ: $6.3m\Omega$)
- Special process technology for high ESD capability
- Special designed for Convertors and power controls
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

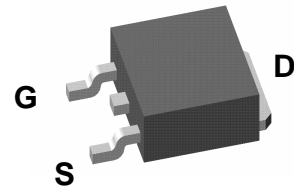


Schematic diagram

TO-252



Marking and pin assignment



TO-252 top view

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	80	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	60	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	140	W
Peak diode recovery voltage	dv/dt	15	V/ns
Derating factor		1.13	W/°C
Single pulse avalanche energy ^(Note 5)	E_{AS}	580	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to- Case ^(Note 2)	$R_{\theta jc}$	1.14	°C/W
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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

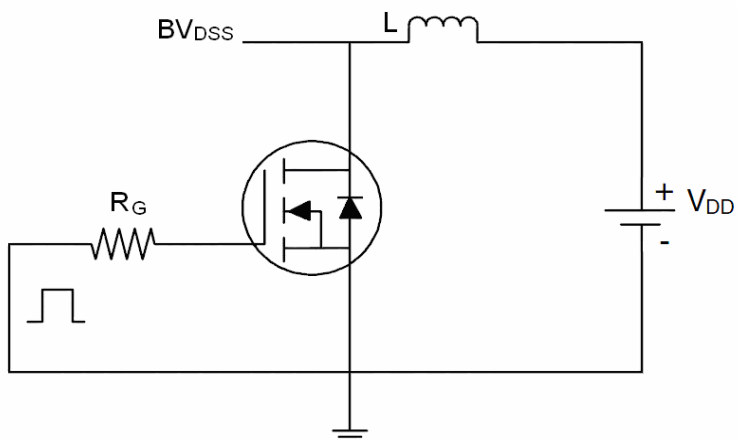
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	80	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=30A$	-	6.3	7.9	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=30A$	-	60	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$		4020		PF
Output Capacitance	C_{oss}			348		PF
Reverse Transfer Capacitance	C_{riss}			290		PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$		17.8		nS
Turn-on Rise Time	t_r			11.8		nS
Turn-Off Delay Time	$t_{d(off)}$			56		nS
Turn-Off Fall Time	t_f			14.6		nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=30A,$ $V_{GS}=10V$		100		nC
Gate-Source Charge	Q_{gs}			20		nC
Gate-Drain Charge	Q_{gd}			30		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	80	A
Reverse Recovery Time	t_{rr}	$T_j=25^\circ\text{C}, I_{SD}=40A, V_{GS}=0V$			36	nS
Reverse Recovery Charge	Q_{rr}	$T_j=25^\circ\text{C}, I_F=75A, di/dt=100A/\mu s$			56	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

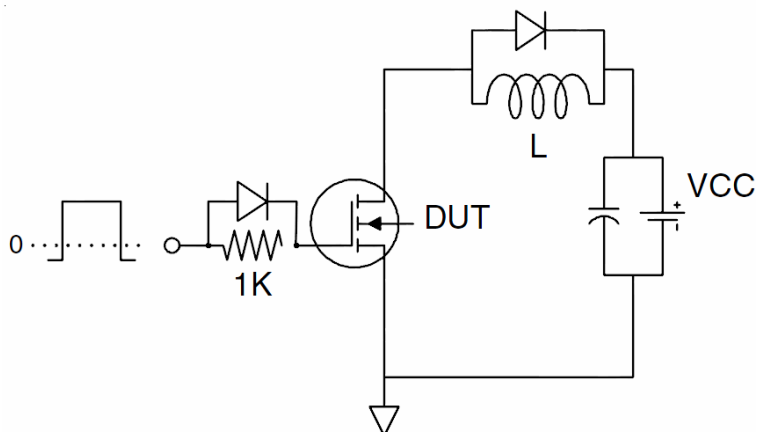
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_j=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, I_D=62A$

Test circuit

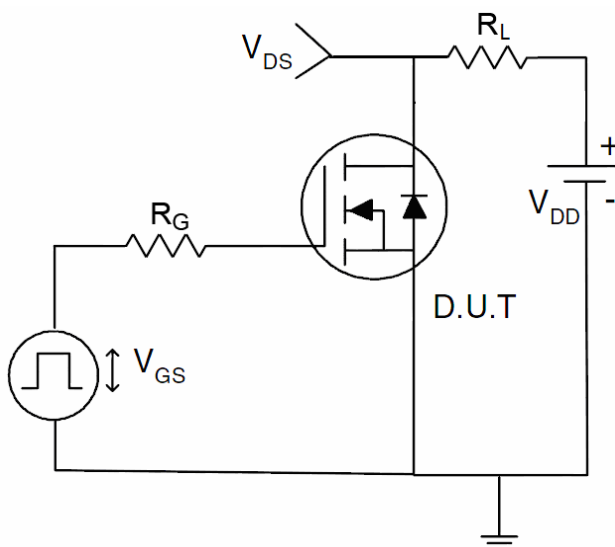
1) E_{AS} test Circuits



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (curves)

Figure1. Safe operating area

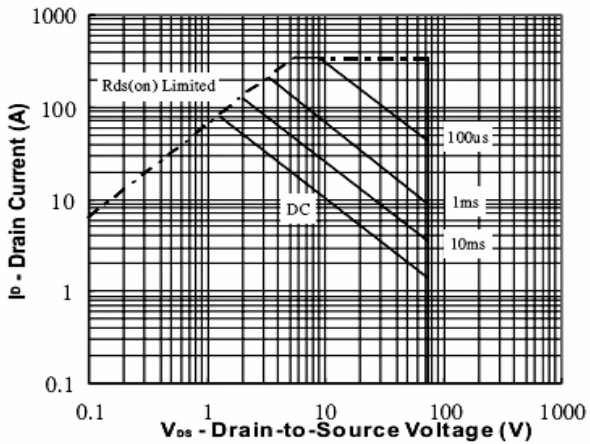


Figure2. Source-Drain Diode Forward Voltage

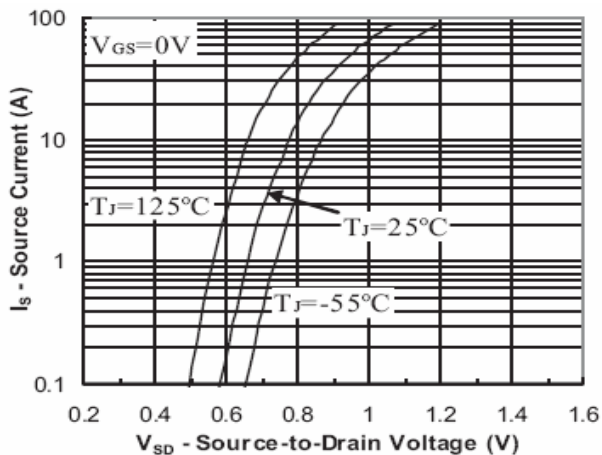


Figure3. Output characteristics

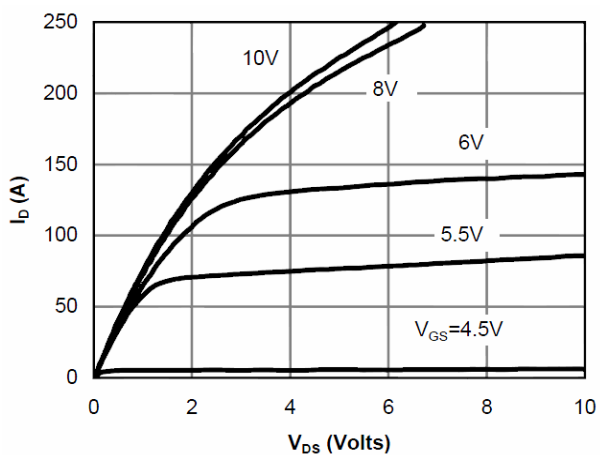


Figure4. Transfer characteristics

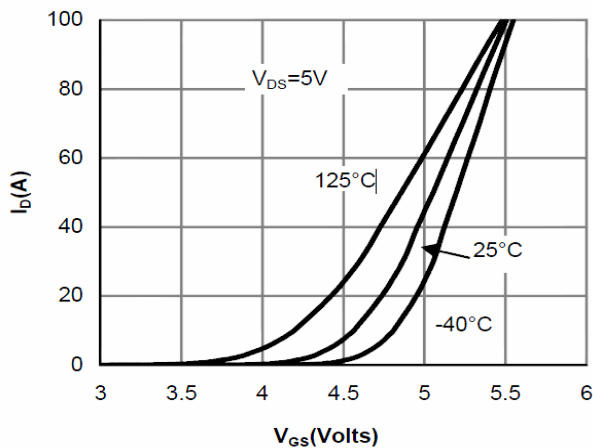


Figure5. Static drain-source on resistance

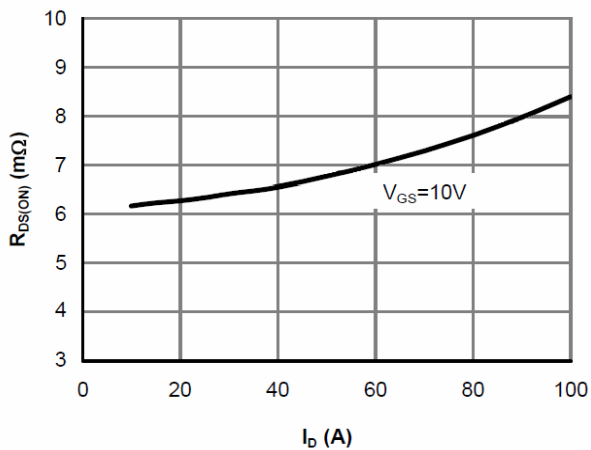


Figure6. $R_{DS(ON)}$ vs Junction Temperature

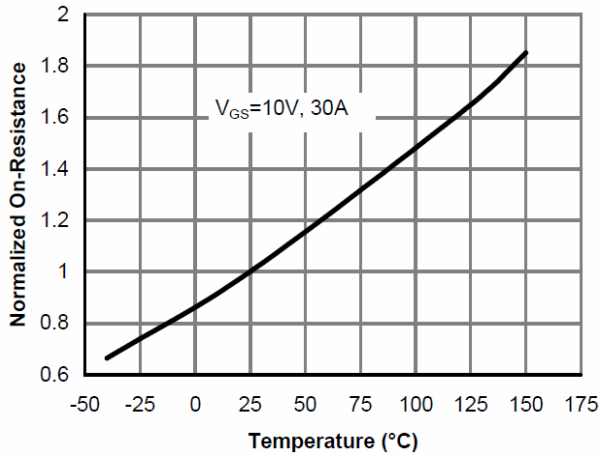


Figure7. BV_{DSS} vs Junction Temperature

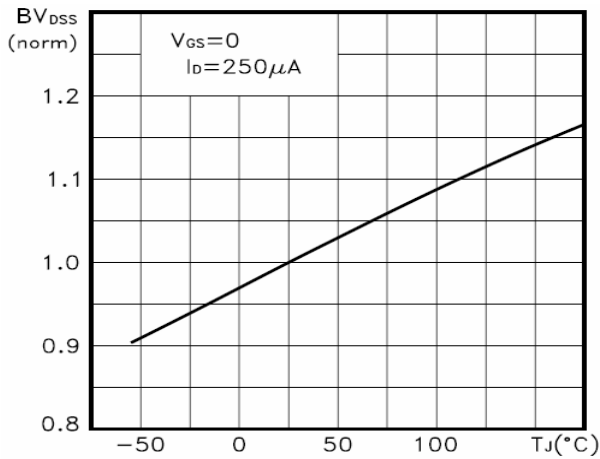


Figure8. $V_{GS(th)}$ vs Junction Temperature

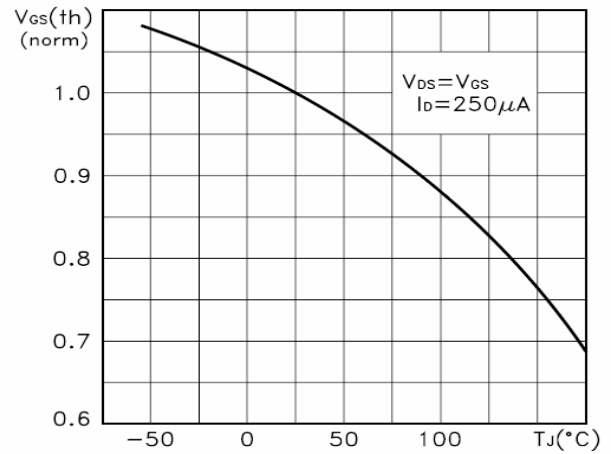


Figure9. Gate charge waveforms

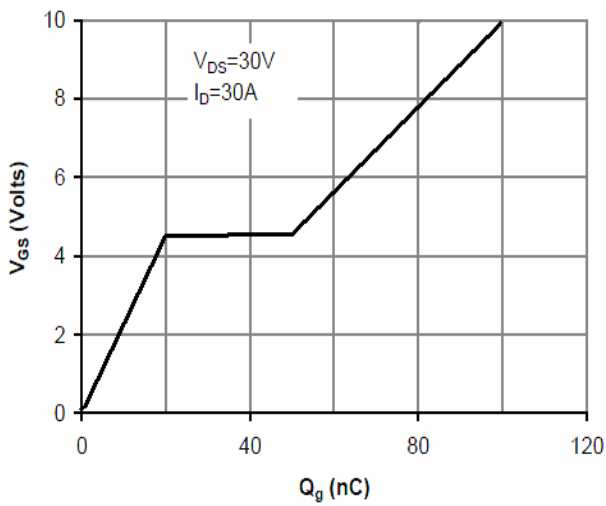
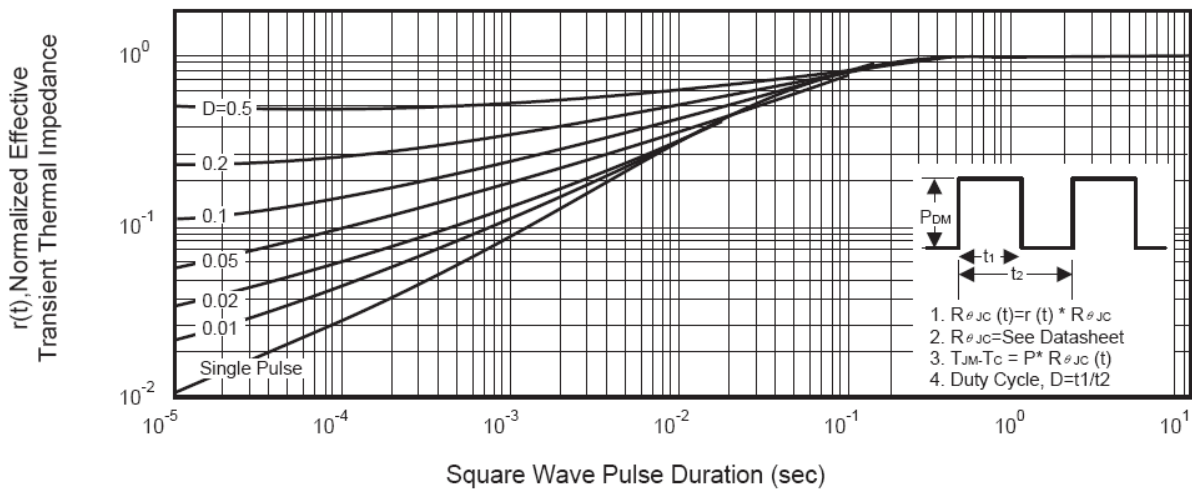
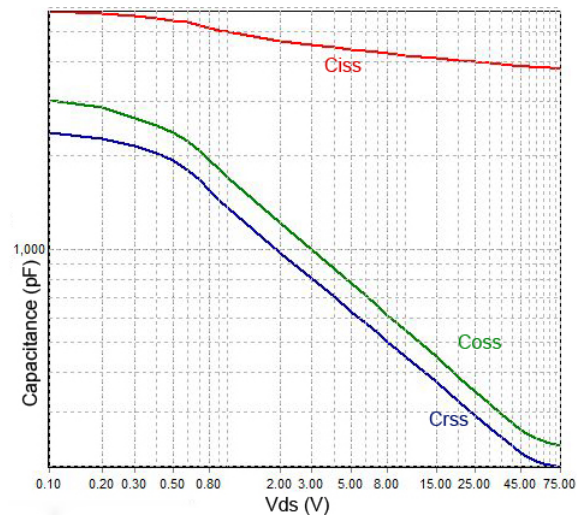
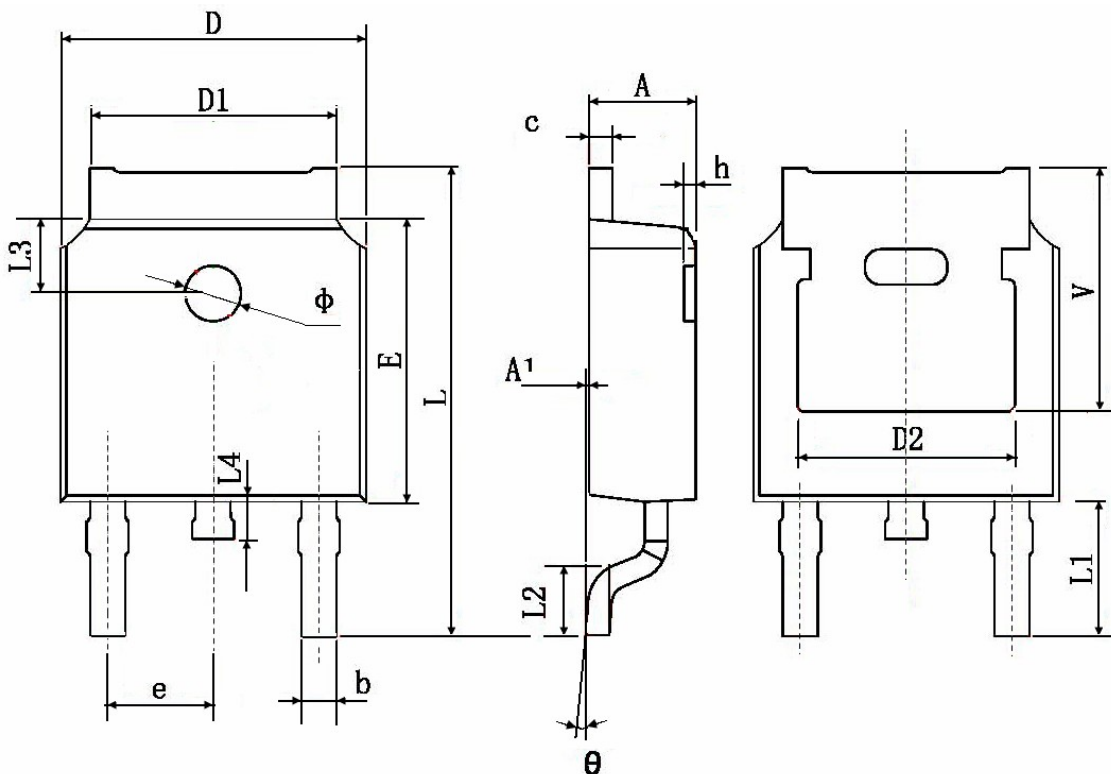


Figure10. Capacitance



Package Information : TO-252



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	