FH1302G6

N-Channel Trench Power MOSFET

Description

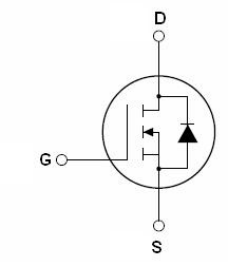
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on state resistance, provide superior switching performance, and with stand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

General Features

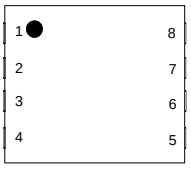
- V_{DS} ≥ 20V , ID=35A
  $R_{DS(ON)}$ =3.0 mΩ (MAX) @V_{GS}=4.5V
  $R_{DS(ON)}$ =4.0 mΩ (MAX) @V_{GS}=2.5V
- Advanced trench cell design
- Low Thermal Resistance

Applications

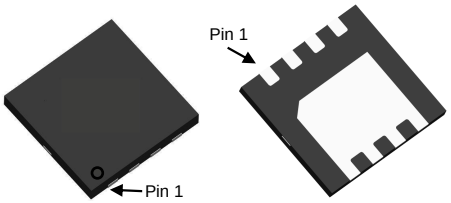
- Motor Drives
- DC-DC Converter



Schematic diagram



Marking and pin Assignment



DFN3.3x3.3-8L top and bottom view

Absolute Maximum Ratings (T_C=25℃ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C = 25 ℃	-	20	V
V_{GS}	Gate-Source Voltage	T_C = 25 ℃	-	± 12	V
I_D*,***	Drain Current	T_C = 25 ℃, V_{GS} = 10 V	-	35	A
I_{DM}*,**,***	Pulsed Source Current	T_C = 25 ℃, V_{GS} = 10 V	-	108	A
P_{tot}*	Total Power Dissipation	T_C = 25 ℃	-	41	W
T_{stg}	Storage Temperature		- 55	150	℃
T_J	Junction Temperature		-	150	℃
I_S	Diode Forward Current	T_C = 25 ℃	-	35	A
$R_{\theta JA}$*	Thermal Resistance- Junction to Ambient		-	62.5	℃ / W
$R_{\theta JC}$*	Thermal Resistance- Junction to Case		-	3	

Notes：

* Surface Mounted on 1 in^2 pad area, t ≤ 10 sec

** Pulse width ≤ 10 μs, duty cycle ≤ 1 %

*** limited by bonding wire

Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	20	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	0.5	-	1	V
I_{DSS}	Zero Gate Voltage Source Current	V_{DS} = 16 V, V_{GS} = 0 V	-	-	1	μA
		T_J = 85 ℃	-	-	30	μA
I_{GSS}	Gate Leakage Current	V_{GS} = ± 12 V, V_{DS} = 0 V	-	-	± 100	nA
$R_{DS(ON)}$[a]	Drain-Source On-State Resistance	V_{GS} = 4.5 V, I_D = 15 A	-	2.5	3.0	mΩ
		V_{GS} = 2.5 V, I_D = 12 A	-	3.5	4.0	
Diode Characteristics						
V_{SD}[a]	Diode Forward Voltage	I_{SD} = 15 A, V_{GS} = 0 V	-	-	1.1	V
t_{rr}	Reverse Recovery Time	I_{SD} = 15 A, dI_{SD}/dt = 100 A/μs	-	66	-	ns
Q_{rr}	Reverse Recovery Charge		-	89	-	nC
Dynamic Characteristics[b]						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 10 V Frequency = 1 MHz	-	6175	-	pF
C_{oss}	Output Capacitance		-	1693	-	
C_{rss}	Reverse Transfer Capacitance		-	1266	-	
t_d(on)	Turn-on Delay Time	V_{DS} = 10 V, V_{GEN} = 10 V, R_G = 4.5 Ω, R_L = 0.6 Ω, I_{DS} = 15 A	-	9.2	-	ns
t_r	Turn-on Rise Time		-	64	-	
t_d(off)	Turn-off Delay Time		-	196	-	
t_f	Turn-off Fall Time		-	83	-	
Gate Charge Characteristics[b]						
Q_g	Total Gate Charge	V_{DS} = 10 V, V_{GS} = 4.5 V, I_{DS} = 15 A	-	80	-	nC
Q_{gs}	Gate-Source Charge		-	10	-	
Q_{gd}	Gate-Drain Charge		-	24	-	

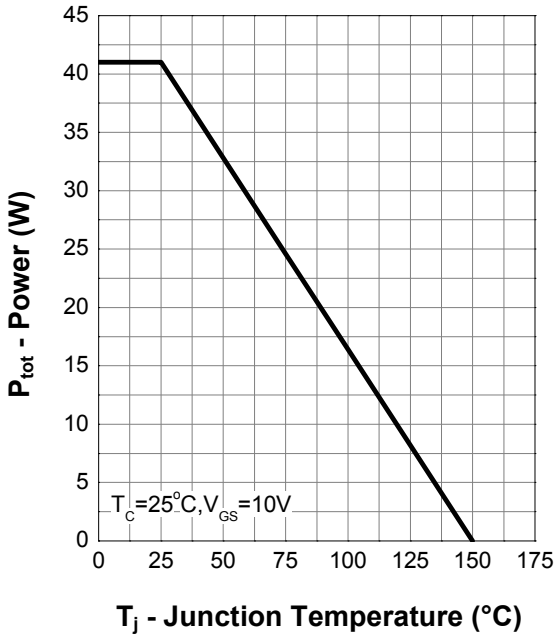
Notes :

a : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2 %

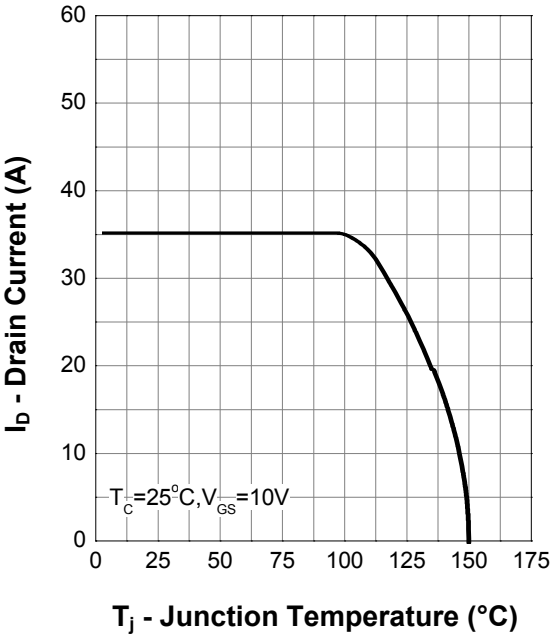
b : Guaranteed by design, not subject to production testing

Typical Characteristics (Cont.)

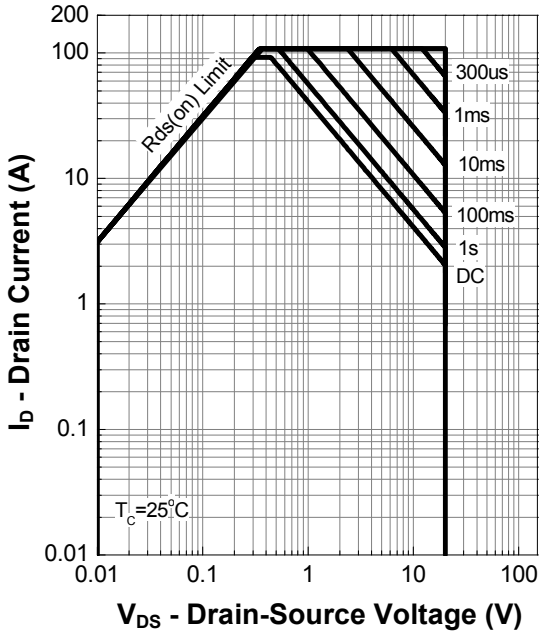
Power Capability



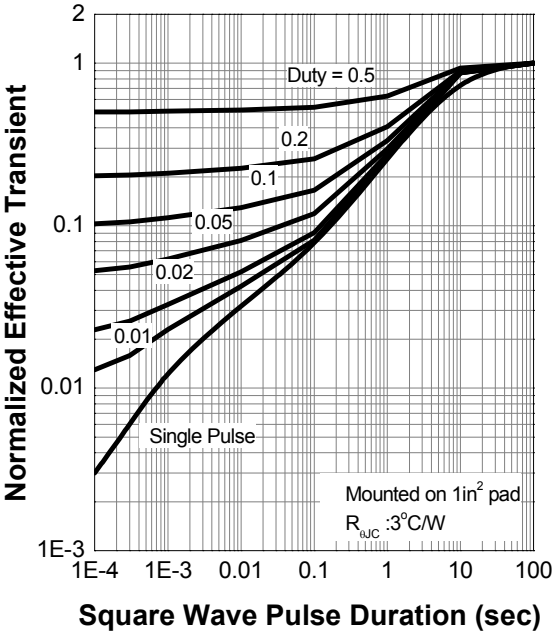
Current Capability



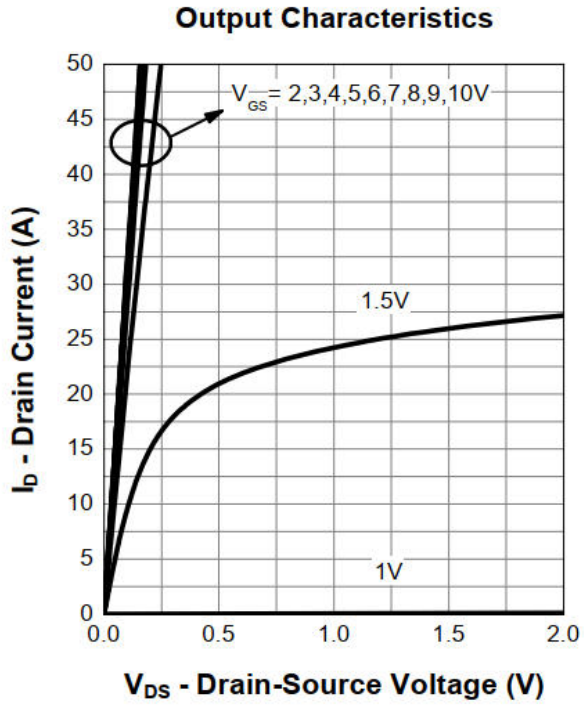
Safe Operation Area

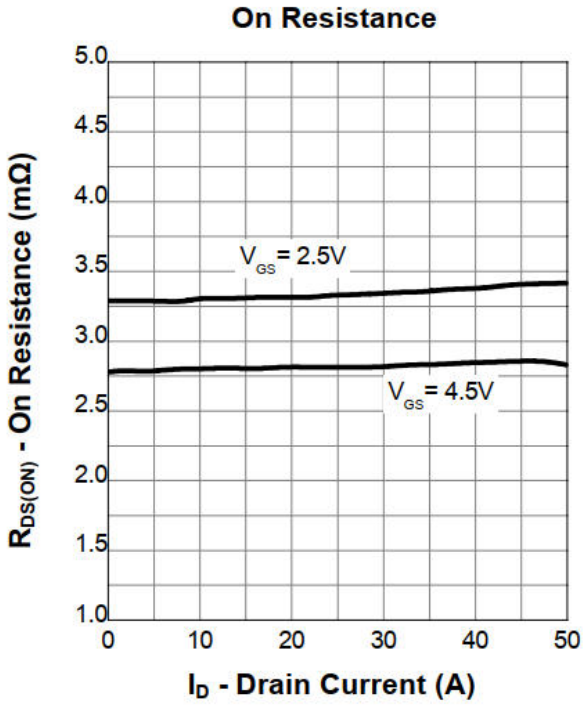


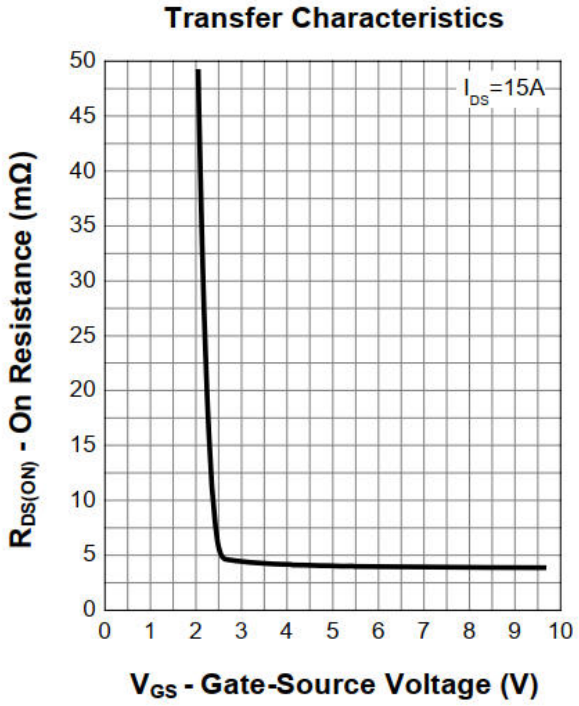
Transient Thermal Impedance

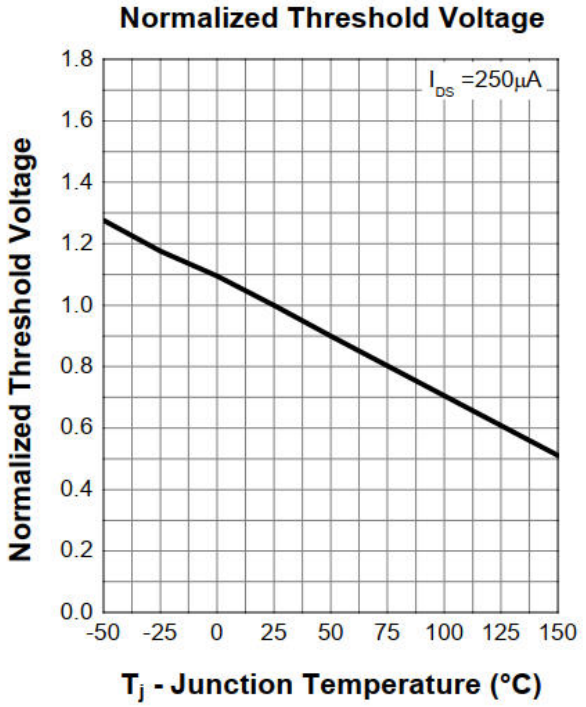


Typical Characteristics (Cont.)

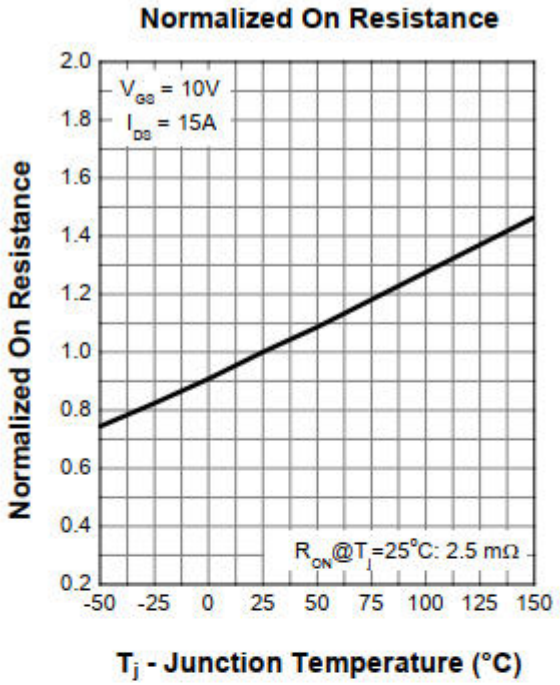


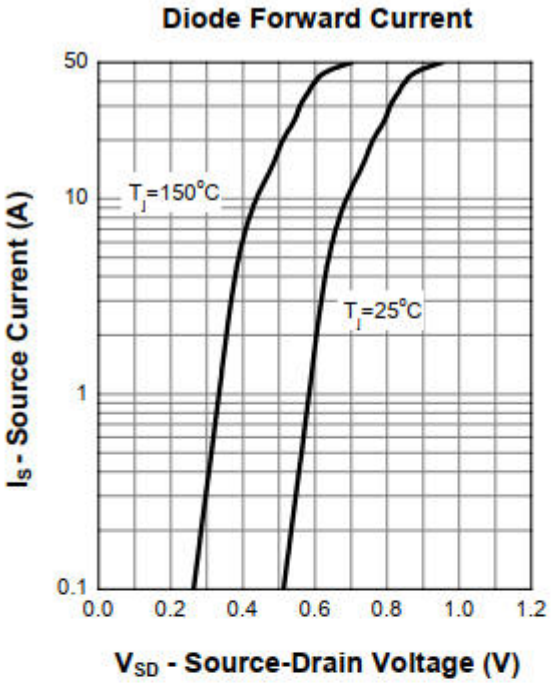


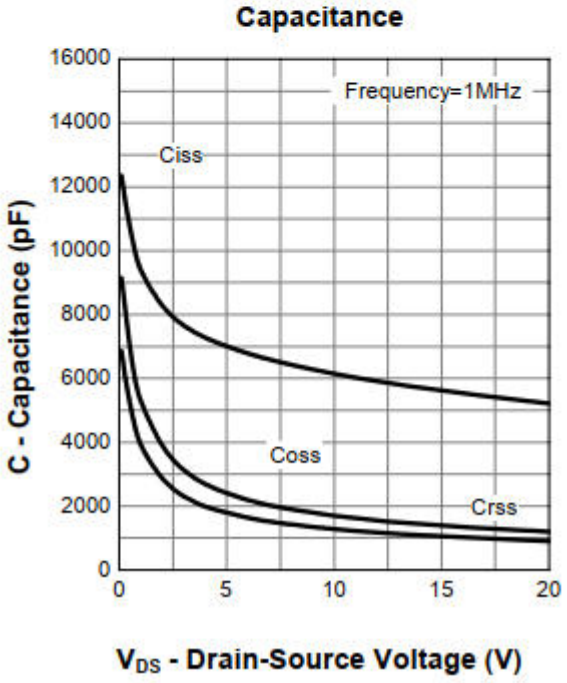


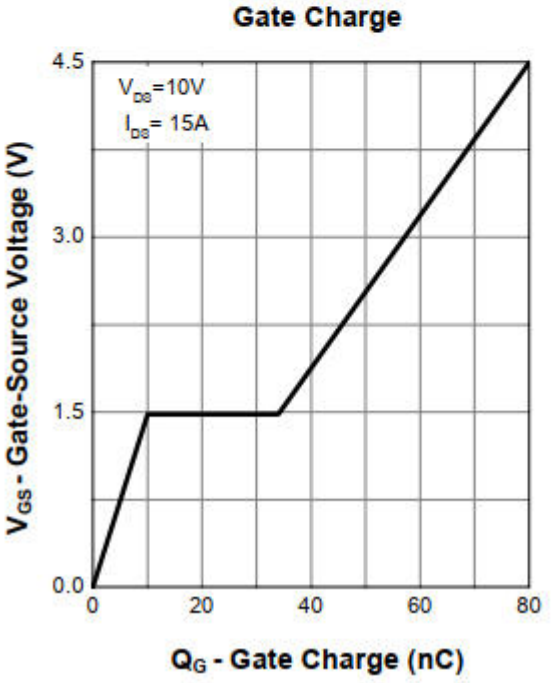


Typical Characteristics (Cont.)

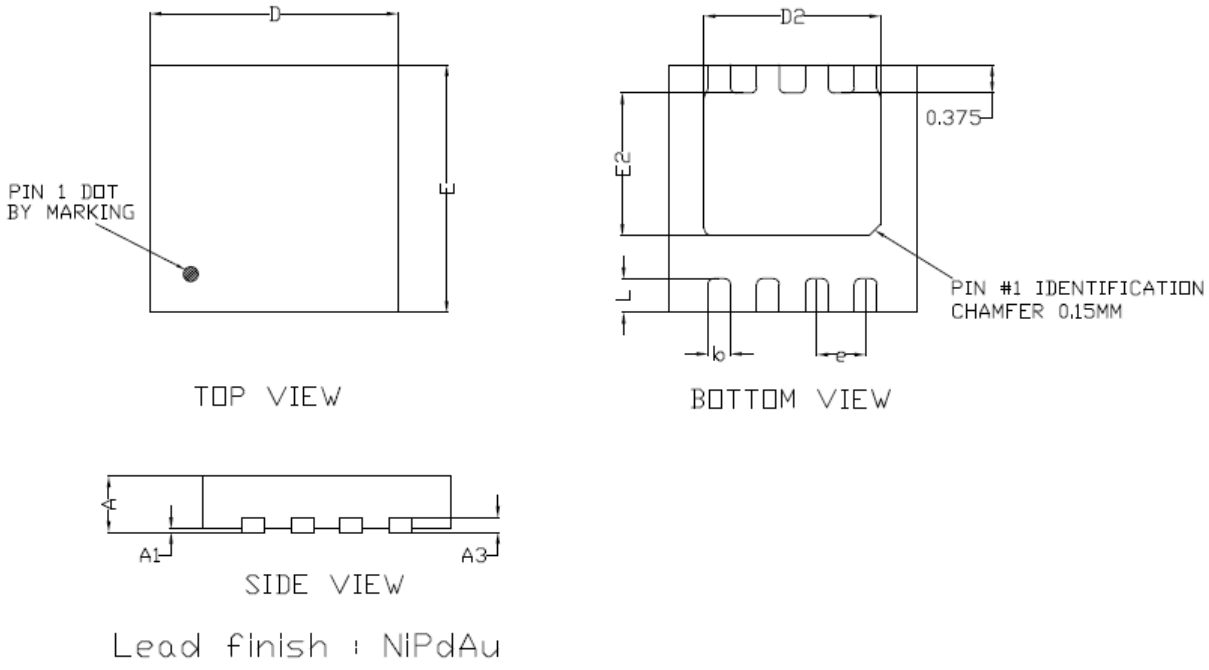








Package Information : DFN3.3*3.3-8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	0.7	0.8
A1	0.00	0.05
A3	0.20 REF	
D	3.20	3.40
E	3.20	3.40
D2	2.30	2.40
E2	1.85	1.95
b	0.25	0.35
L	0.35	0.55
e	0.65 BSC	