

# FH3404TL4

## N-Channel Trench Power MOSFET

### Description

The FH3404TL4 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

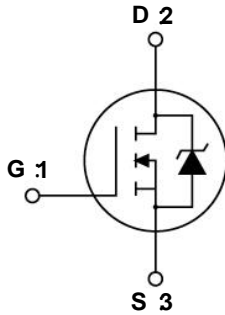
### Application

- Load Switch
- PWM Application
- Battery Management

### Features

Parameter	Typ.	Unit
$V_{DS}$	40	V
$I_D$ (@ $V_{GS} = 10V$ )	140	A
$R_{DS(ON)}$ (@ $V_{GS} = 10V$ ) (Typ)	2.4	m $\Omega$
$R_{DS(ON)}$ (@ $V_{GS} = 4.5V$ ) (Typ)	3.1	m $\Omega$

- Advanced Trench Technology
- Provide Excellent  $R_{DS(ON)}$  and Low Gate Charge



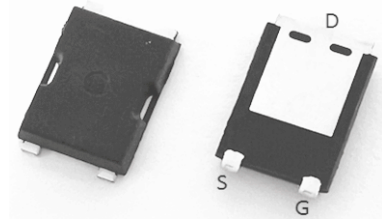
Schematic diagram

Top view



Marking and pin assignment

TOLL-4L



Top view

Bottom View

### Absolute Maximum Ratings (T<sub>c</sub>=25°C unless otherwise specified)

Symbol	Parameter	Value	Units
$V_{DSS}$	Drain-Source Voltage	40	V
$V_{GSS}$	Gate-Source Voltage	±20	V
$I_D$	Continuous Drain Current	T <sub>c</sub> = 25°C	140
		T <sub>c</sub> = 100°C	91
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	420	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note2</sup>	463	mJ
$P_D$	Power Dissipation	T <sub>c</sub> = 25°C	63
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2	°C/W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	°C

**Electrical Characteristics** ( $T_C=25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=32V, V_{GS}=0V,$	-	-	1.0	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.6	2	V
$R_{DS(on)}$	Static Drain-Source on-Resistance note3	$V_{GS}=10V, I_D=20A$	-	2.4	2.9	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$	-	3.1	3.7	
$g_{FS}$	Forward Transconductance	$V_{DS}=5V, I_D=20A$	-	15	-	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=20V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	4806	-	pF
$C_{oss}$	Output Capacitance		-	415	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	384	-	pF
$R_g$	Gate resistance	-	-	2.4	-	$\Omega$
<b>Switching Characteristics</b>						
$Q_g$	Total Gate Charge	$V_{DS}=20V, I_D=20A,$ $V_{GS}=10V$	-	100	-	nC
$Q_{gs}$	Gate-Source Charge		-	10	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	26	-	nC
$V_{plateau}$	Gate plateau voltage		-	2.6	-	V
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=20V, V_{GS}=10V$ $RL=0.5\Omega, R_{GEN}=3\Omega,$	-	20	-	ns
$t_r$	Turn-on Rise Time		-	108	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	95	-	ns
$t_f$	Turn-off Fall Time		-	111	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	140	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	420	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=10A$	-	-	1.2	V

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition:  $T_J=25^\circ\text{C}, V_{DD}=30V, V_G=10V, R_G=25\Omega, L=0.5\text{mH}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$ , Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: On-Region Characteristics

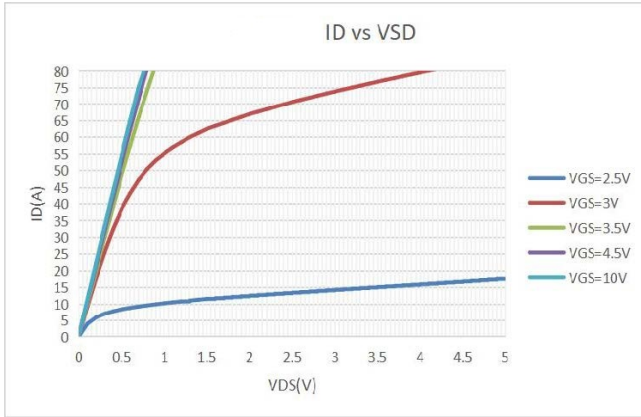


Figure 2: Transfer Characteristics

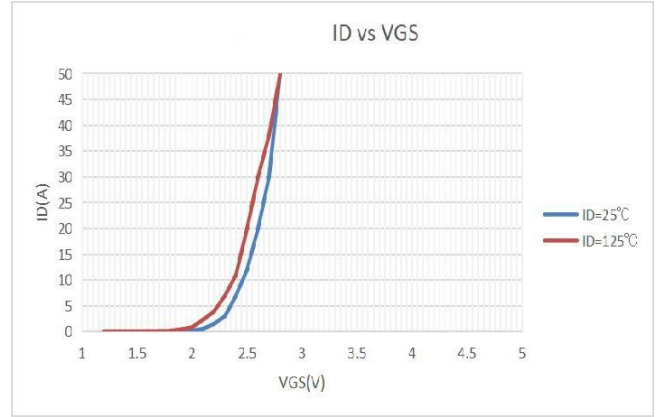


Figure 3: On-resistance vs. Drain Current and Gate Voltage

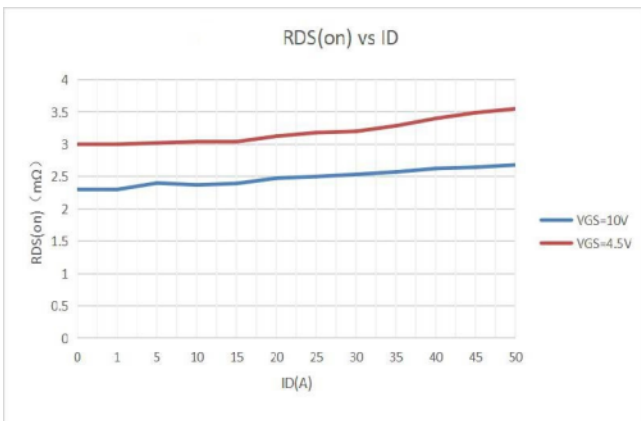


Figure 4: On-Resistance vs. Gate-Source Voltage



Figure 5: On-Resistance vs. Junction Temperature

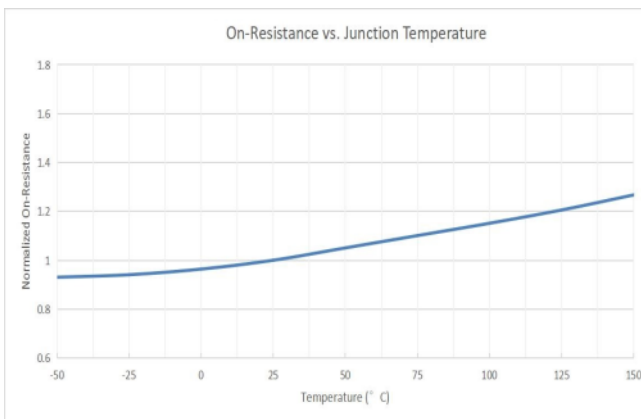
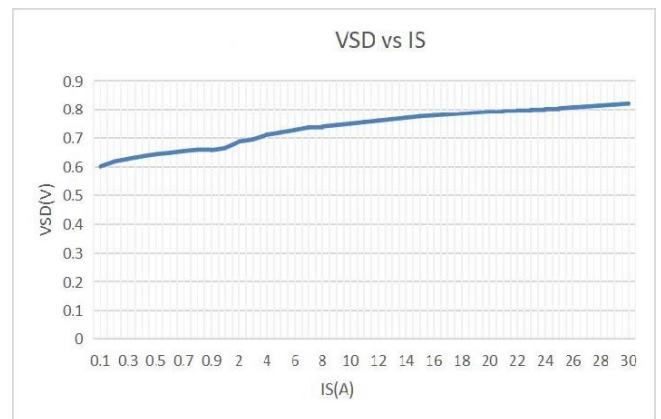
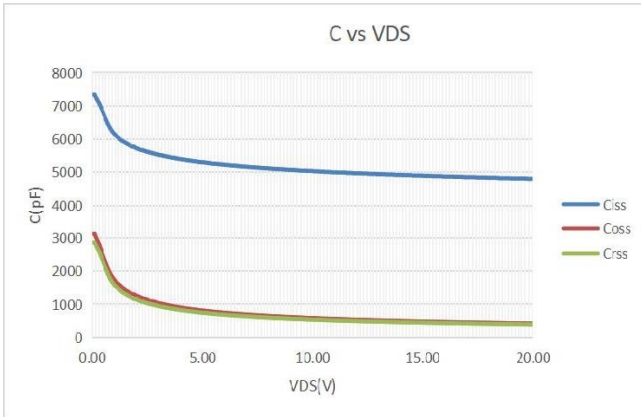


Figure 6: Body-Diode Characteristics

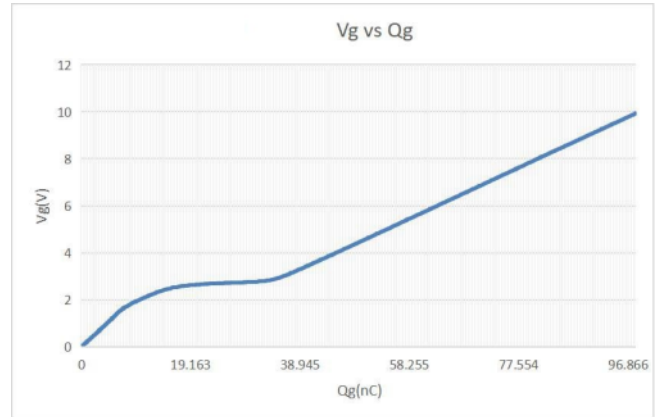


## Typical Performance Characteristics

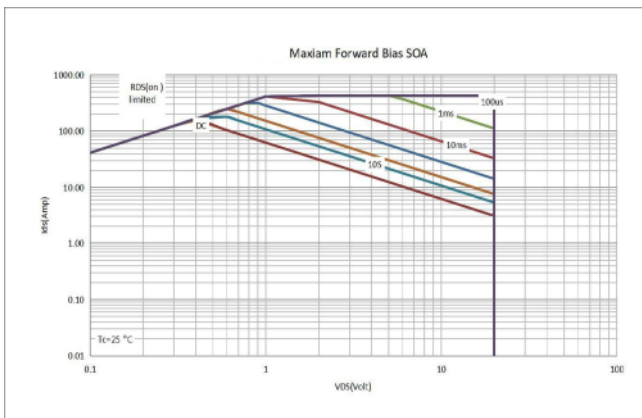
**Figure7:** Capacitance Characteristics C(pF)



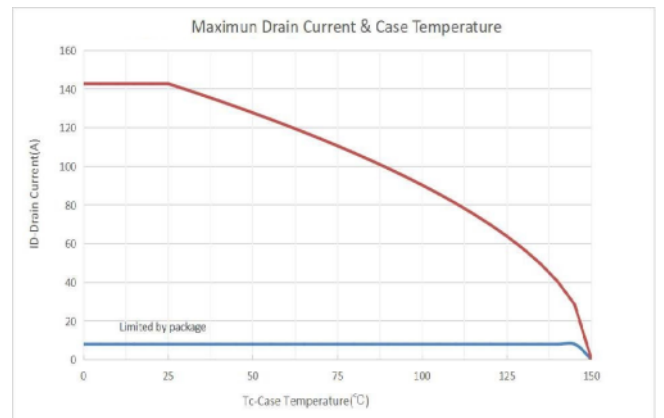
**Figure 8:** Gate-Charge Characteristics



**Figure9:** Maximum Forward Biased Safe Operating Area



**Figure10:** Current De-rating



Test Circuit

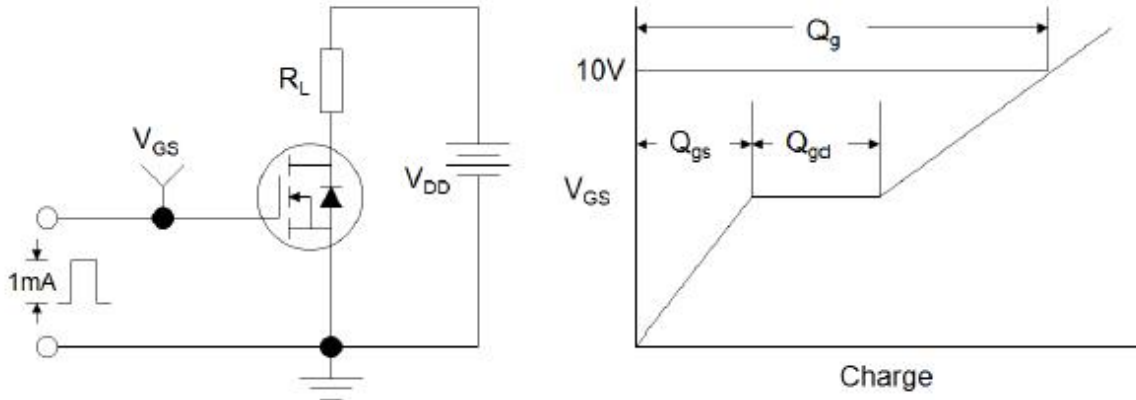


Figure1:Gate Charge Test Circuit & Waveform

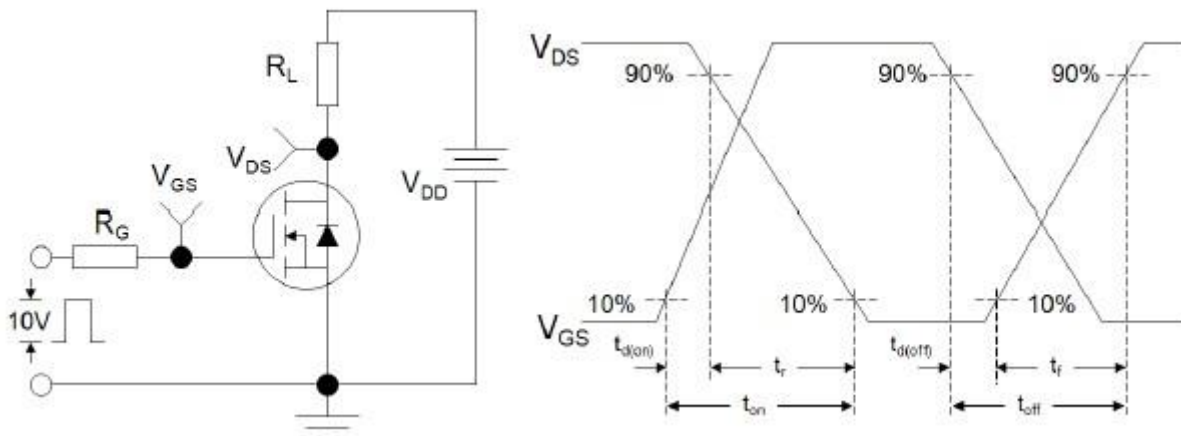


Figure 2: Resistive Switching Test Circuit & Waveforms

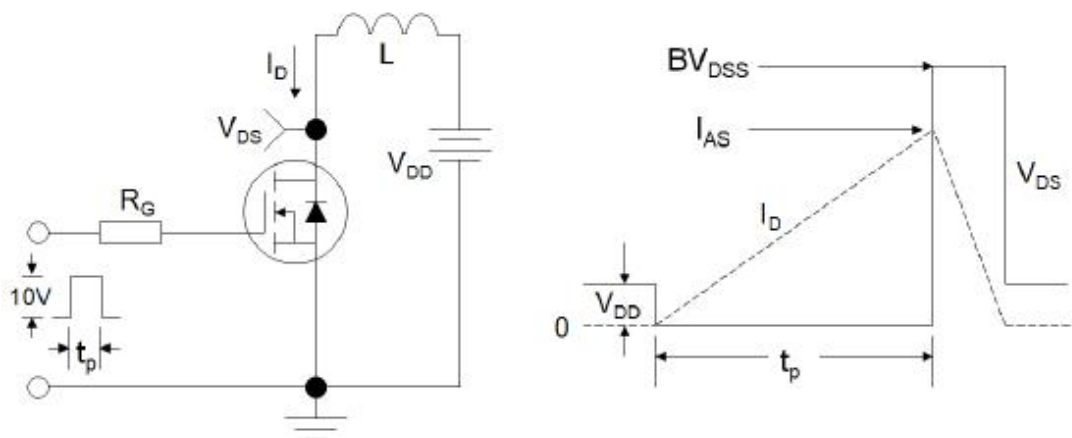


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

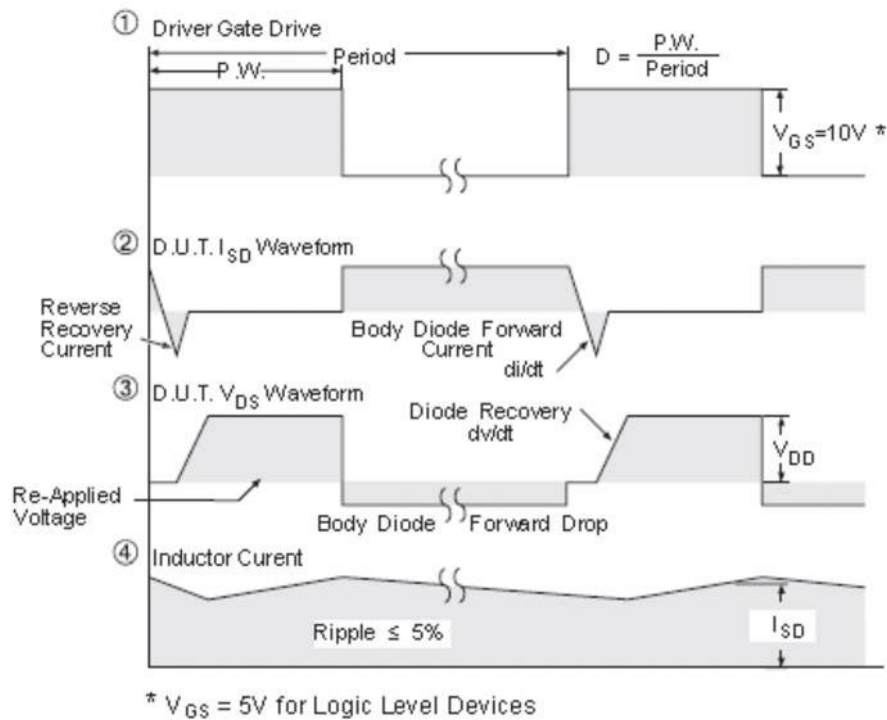
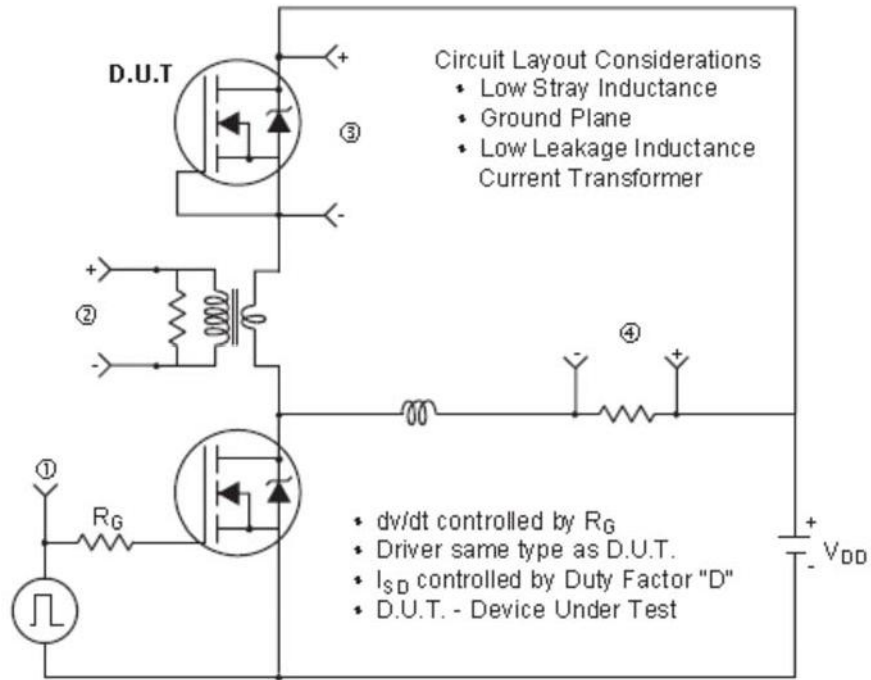


Figure 4: Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms (For N-channel)

