

FH3504TL4

N-Channel Trench Power MOSFET

Description

The FH3504TL4 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

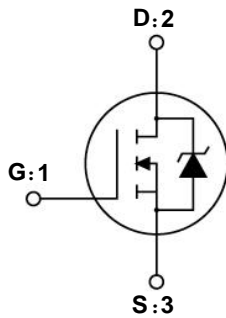
Application

- Load Switch
- PWM Application
- Battery Management

Features

Parameter	Typ.	Unit
V_{DS}	40	V
I_D (@ $V_{GS} = 10V$)	150	A
$R_{DS(ON)}$ (@ $V_{GS} = 10V$) (Typ)	2.1	m Ω
$R_{DS(ON)}$ (@ $V_{GS} = 4.5V$) (Typ)	2.7	m Ω

- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge



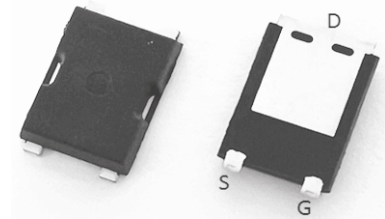
Schematic diagram

Top view



Marking and pin assignment

TOLL-4L



Top view

Bottom View

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	40	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	150
		$T_C = 100^\circ C$	95
I_{DM}	Pulsed Drain Current ^{note1}	450	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	463	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	63
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=32V, V_{GS}=0V,$	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.6	2	V
$R_{DS(on)}$	Static Drain-Source on-Resistance <small>note3</small>	$V_{GS}=10V, I_D=20A$	-	2.1	2.5	m Ω
		$V_{GS}=4.5V, I_D=20A$	-	2.7	3.2	
g_{FS}	Forward Transconductance	$V_{DS}=5V, I_D=20A$	-	15	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=20V, V_{GS}=0V,$ $f=1.0MHz$	-	4672	-	pF
C_{oss}	Output Capacitance		-	411	-	pF
C_{rss}	Reverse Transfer Capacitance		-	381	-	pF
R_g	Gate resistance		-	2.4	-	Ω
Switching Characteristics						
Q_g	Total Gate Charge	$V_{DS}=20V, I_D=20A,$ $V_{GS}=10V$	-	99	-	nC
Q_{gs}	Gate-Source Charge		-	11	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	22	-	nC
$V_{plateau}$	Gate plateau voltage		-	2.7	-	V
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=20V, V_{GS}=10V$ $RL=2\Omega, R_{GEN}=3\Omega,$	-	18	-	ns
t_r	Turn-on Rise Time		-	118	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	89	-	ns
t_f	Turn-off Fall Time		-	108	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	150	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	450	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=10A$	-	-	1.2	V

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}, V_{DD}=30V, V_G=10V, R_G=25\Omega, L=0.5mH$

3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: On-Region Characteristics

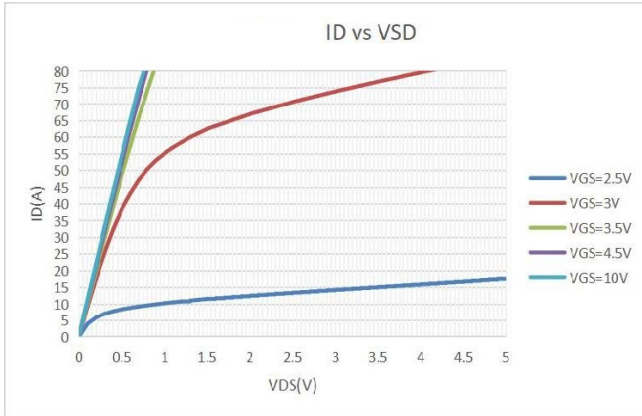


Figure 2: Transfer Characteristics

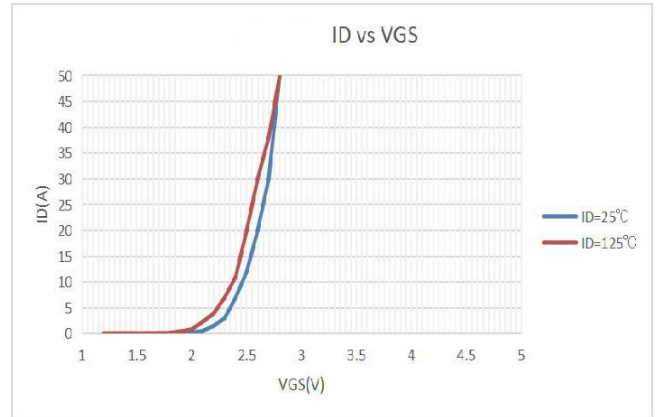


Figure 3: On-resistance vs. Drain Current and Gate Voltage

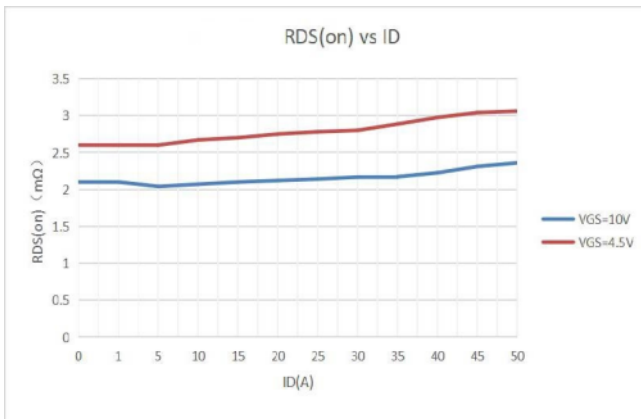


Figure 4: On-Resistance vs. Gate-Source Voltage

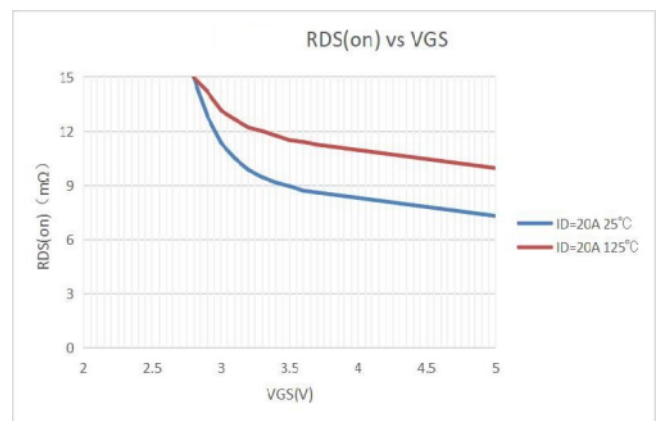


Figure 5: On-Resistance vs. Junction Temperature

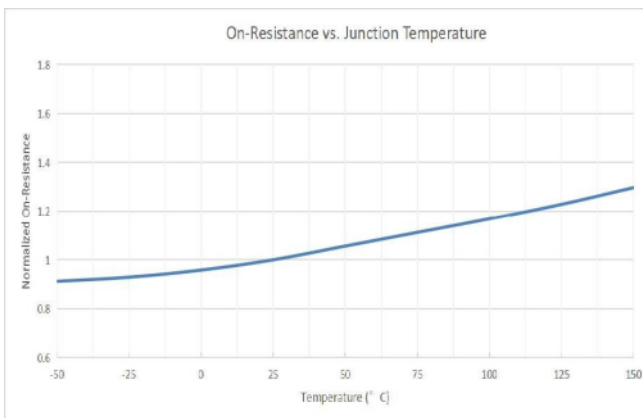
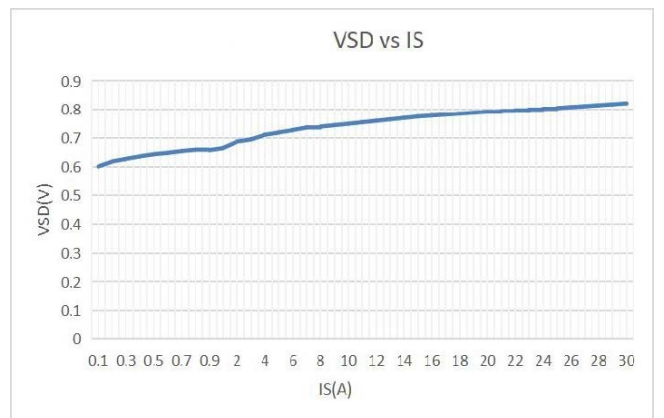


Figure 6: Body-Diode Characteristics



Typical Performance Characteristics

Figure7: Capacitance Characteristics C(pF)

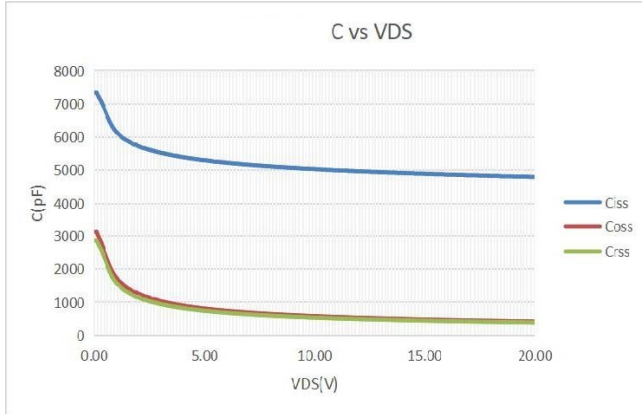


Figure 8: Gate-Charge Characteristics

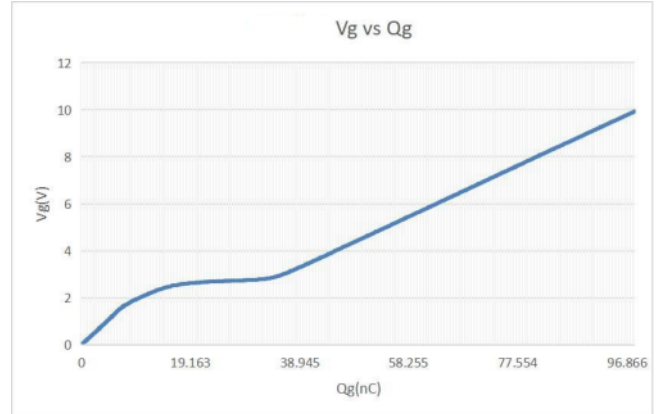


Figure9: Maximum Forward Biased Safe Operating Area

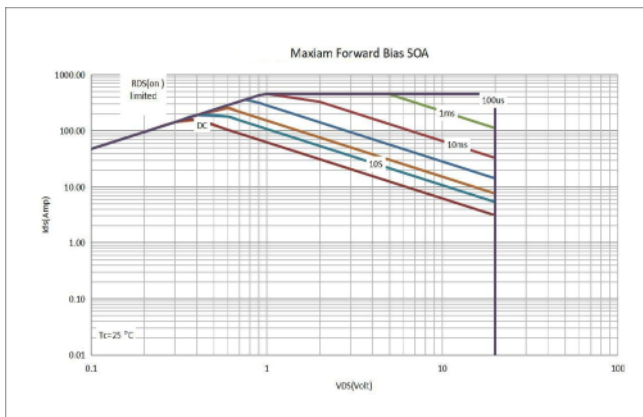
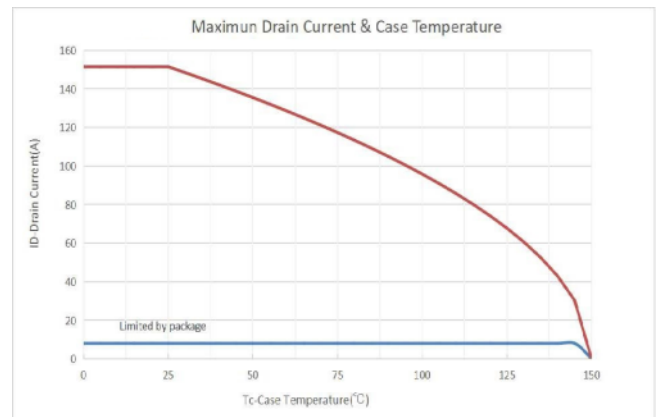


Figure10: Current De-rating



Test Circuit

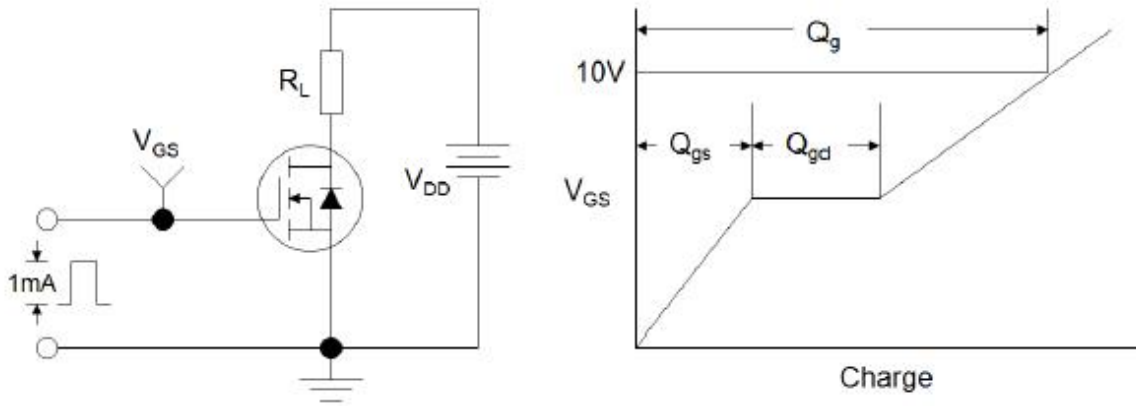


Figure 1: Gate Charge Test Circuit & Waveform

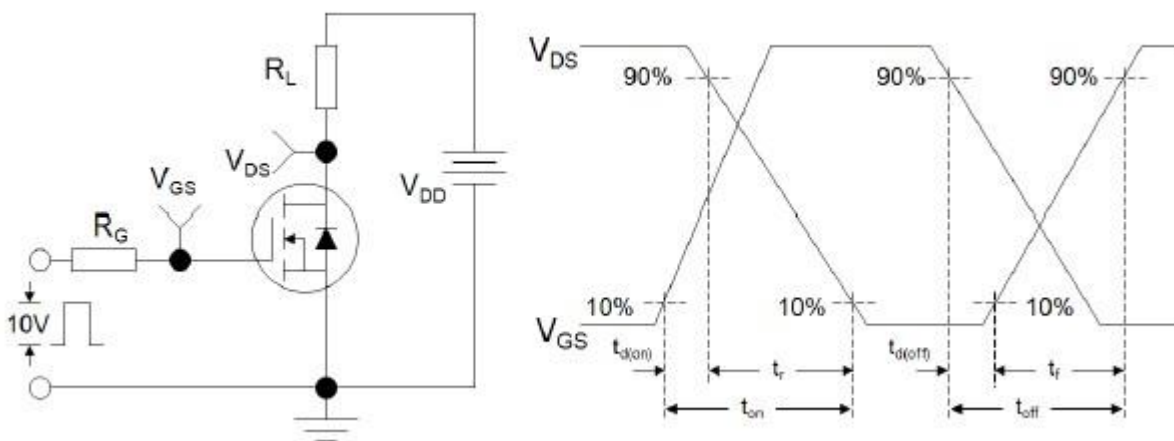


Figure 2: Resistive Switching Test Circuit & Waveforms

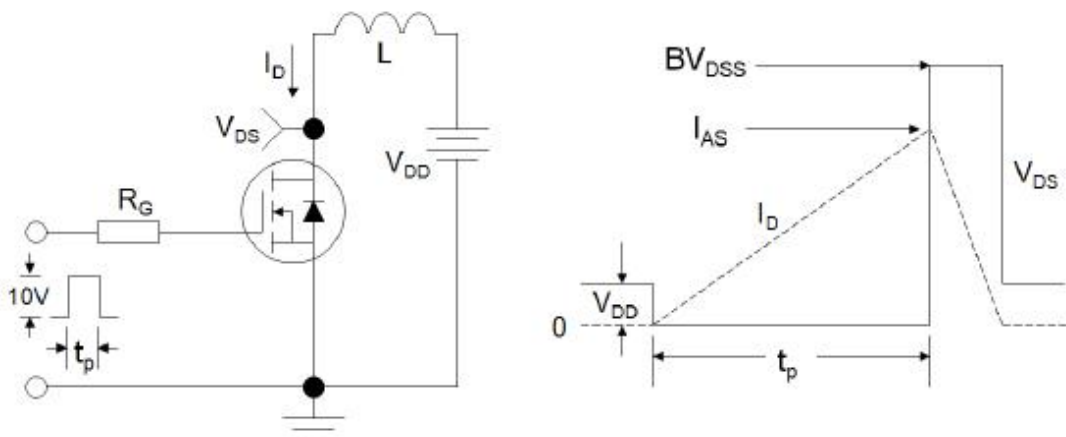
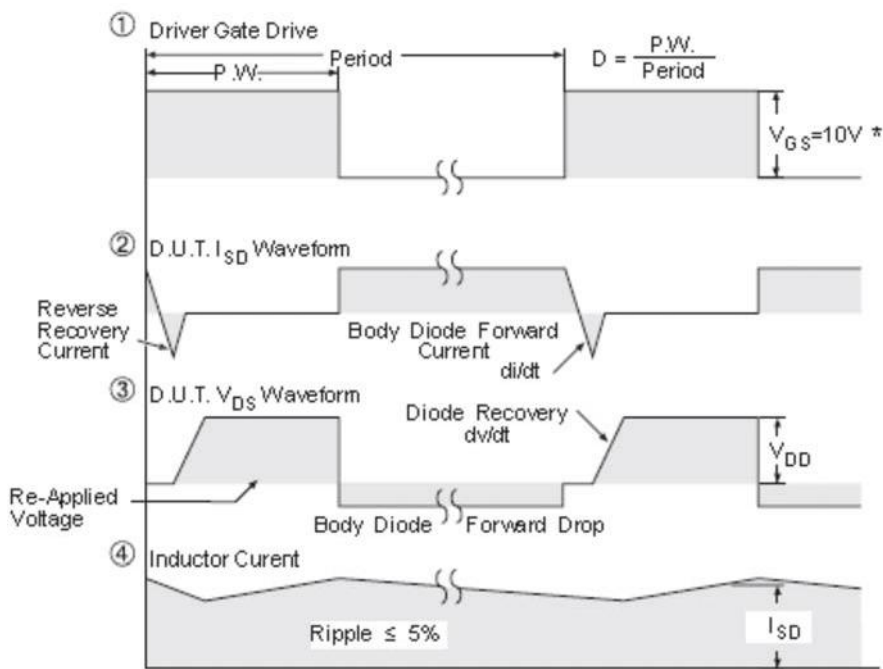
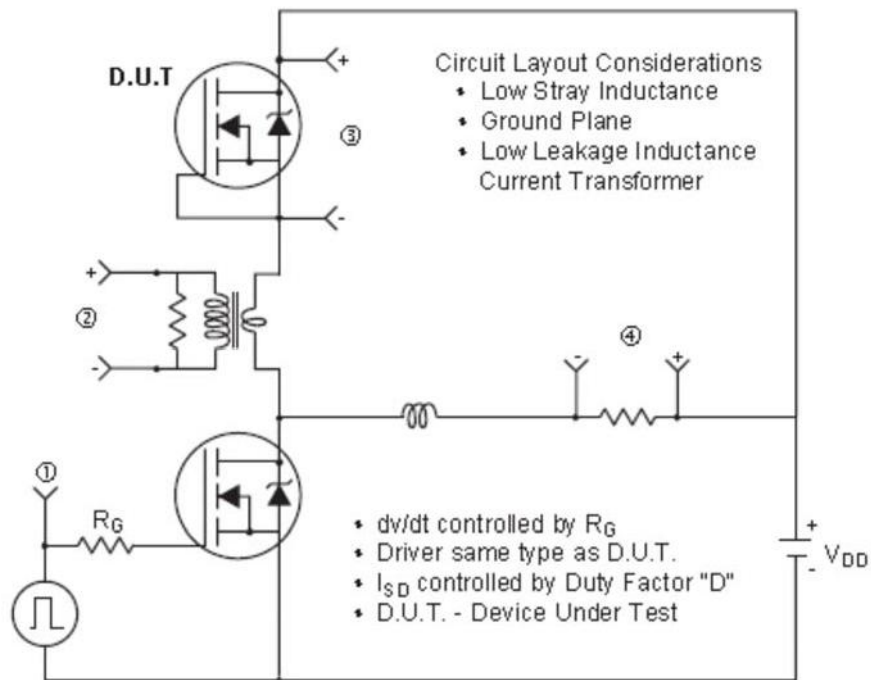


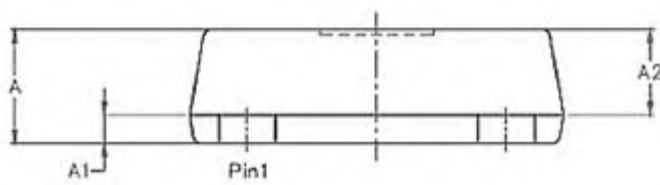
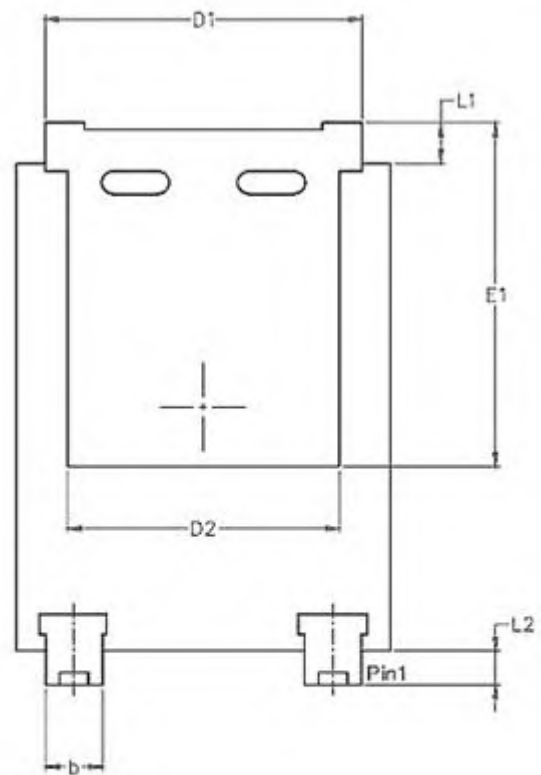
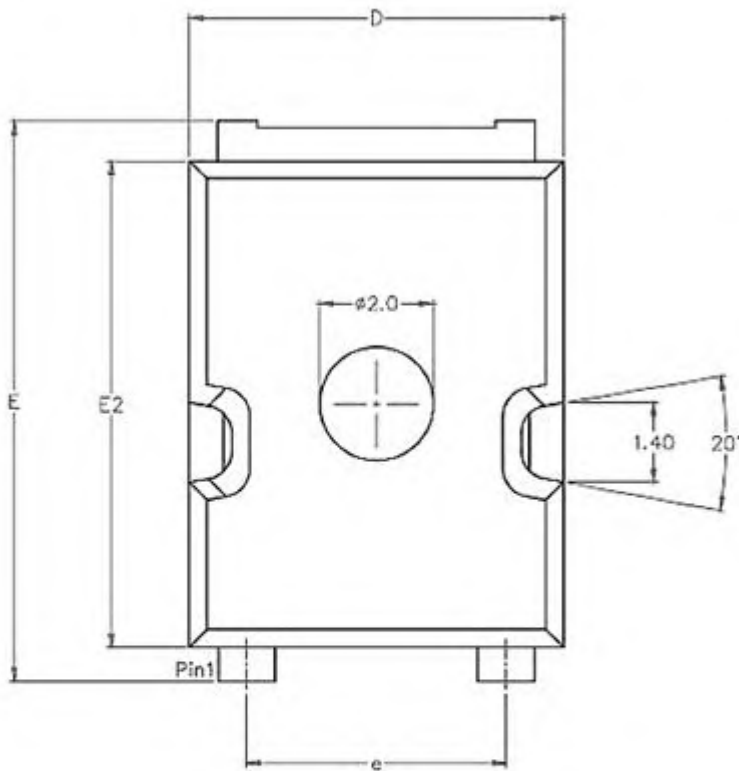
Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms



* $V_{GS} = 5V$ for Logic Level Devices

Figure 4: Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package Information:TOLL-4L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.95	2.00	2.05
A1	0.45	0.50	0.55
A2	1.45	1.50	1.55
b	0.95	1.00	1.05
D	6.55	6.60	6.65
E	9.85	9.90	9.95
D1	5.55	5.60	5.65
D2	4.75	4.80	4.85
E1	6.00	6.05	6.10
E2	8.55	8.60	8.65
e	4.54	4.57	4.60
L1	0.65	0.70	0.75
L2	0.55	0.60	0.65