FH3015PS

N-Channel Enhancement Mode Power MOSFET

General Description

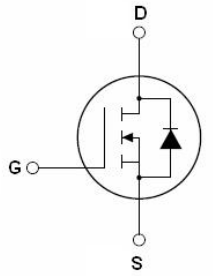
This N channel SGT MOSFET has been designed to very low on-state resistance (RDSON) and yet maintain superior switching performance, especially for high efficiency power management applications.

Applications

- DC-DC Conversion
- Power Tools
- Motor Driving
- Power Management

Features

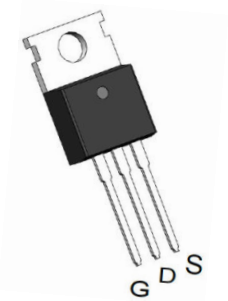
- VDS = 150V, I_D = 100A
  $R_{DS(ON)}$ (Typ)：6.3 mΩ @ VGS = 10V
- N-channel, optimized for high-speed smooth switching
- Excellent Gate Charge ×$R_{DS(ON)}$ (FOM)
- Very low on-resistance



Schematic diagram

TO-220

Marking and pin Assignment



TO-220 top view

Maximum Ratings (at T_j = 25°C, unless otherwise specified)

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C = 25 ℃	150	-	V
V_{GS}	Gate-Source Voltage	T_C = 25 ℃	-	±20	V
I_D* ***	Drain Current (DC)	T_C = 25 ℃, V_{GS} = 10 V	-	100	A
I_{DM}**,***	Drain Current (Pulsed)	T_C = 25 ℃, V_{GS} = 10 V	-	400	A
P_{tot}	Drain power dissipation	T_C = 25 ℃	-	210	W
T_{stg}	Storage Temperature		-55	150	℃
T_J	Junction Temperature		-	150	℃
I_S	Continuous-Source Current	T_C = 25 ℃	-	100	A
E_{AS}	Single Pulsed Avalanche Energy	V_{DD}=50 V , L=0.5mH R_G=25Ω	-	506	mJ
$R_{\theta JA}$	Thermal Resistance- Junction to Ambient ****		-	60	℃/W
$R_{\theta JC}$	Thermal Resistance- Junction to Case		-	0.5	℃/W

Notes：

* Surface Mounted on minimum footprint pad area.

** Pulse width ≤ 300 μs, duty cycle ≤ 2 %

*** Maximum current rating is package limited.

**** Surface mounted on 1in2 FR-4 board.

Electrical Characteristics

at Tj = 25°C, unless otherwise specified

Static Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
$V_{(BR)DSS}$	Drain-source breakdown voltage	150	-	-	V	V_{GS}=0V, I_D=250μA
$V_{(GS)th}$	Gate threshold voltage	2	3	4	V	V_{DS}=V_{GS}, I_D=250μA
I_{DSS}	Zero gate voltage drain current	-	-	1	μA	V_{DS}=150V, V_{GS}=0V, T_j=25°C
I_{GSS}	Gate-source leakage current	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
$R_{DS(on)}$	Drain-source on-state resistance	-	6.3	7.4	mΩ	V_{GS}=10V, I_D=20A, T_j=25°C
R_G	Gate resistance	-	2.4	-	Ω	V_{DD}=0V,V_{GS}=0V,F=1MHz
g_{fs}	Transconductance		80		S	V_{DS}=5V, I_D=20A

Dynamic Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
C_{iss}	Input capacitance	-	5240	-	pF	V_{GS}=0V, V_{DS}=75V, f=1MHz
C_{oss}	Output capacitance	-	412	-	pF	V_{GS}=0V, V_{DS}=75V, f=1MHz
C_{rss}	Reverse transfer capacitance	-	10	-	pF	V_{GS}=0V, V_{DS}=75V, f=1MHz
$t_{d(on)}$	Turn-on delay time	-	22	-	ns	V_{DD}=75V, V_{GS}=10V, I_D=100A, R_G=1.6Ω
t_r	Rise time	-	115	-	ns	V_{DD}=75V, V_{GS}=10V, I_D=100A, R_G=1.6Ω
$t_{d(off)}$	Turn-off delay time	-	44	-	ns	V_{DD}=75V, V_{GS}=10V, I_D=100A, R_G=1.6Ω
t_f	Fall time	-	105	-	ns	V_{DD}=75V, V_{GS}=10V, I_D=100A, R_G=1.6Ω

Gate Charge Characteristics

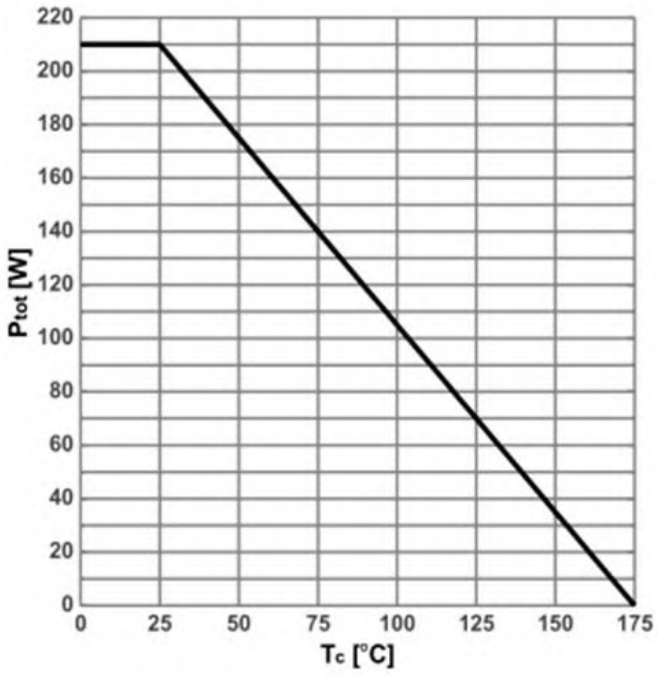
Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
Q_{gs}	Gate to source charge	-	18	-	nC	V_{DD}=75V, I_D=20A, V_{GS}=0 to 10V
Q_{gd}	Gate to drain charge	-	10	-	nC	V_{DD}=75V, I_D=20A, V_{GS}=0 to 10V
Q_g	Gate charge total	-	72	-	nC	V_{DD}=75V, I_D=20A, V_{GS}=0 to 10V
$V_{plateau}$	Gate plateau voltage	-	3.4	-	V	V_{DD}=75V, I_D=20A, V_{GS}=0 to 10V

Reverse Diode Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{SD}	Diode forward voltage	-	0.76	-	V	V_{GS}=0V, I_F=10A, T_f=25°C
t_{rr}	Reverse recovery time	-	45	-	ns	V_R=75V, I_F=100A, di_F/dt=100A/μs
Q_{rr}	Reverse recovery charge	-	12	-	nC	V_R=75V, I_F=100A, di_F/dt=100A/μs
I_{rrm}	Peak reverse recovery current	-	1.2	-	A	V_R=75V, I_F=100A, di_F/dt=100A/μs

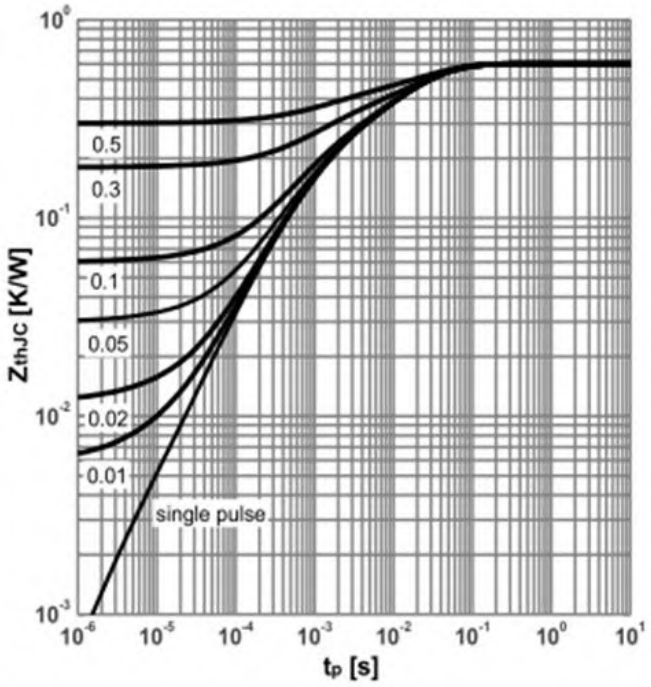
Electrical Characteristics Diagrams

Diagram 1: Power dissipation



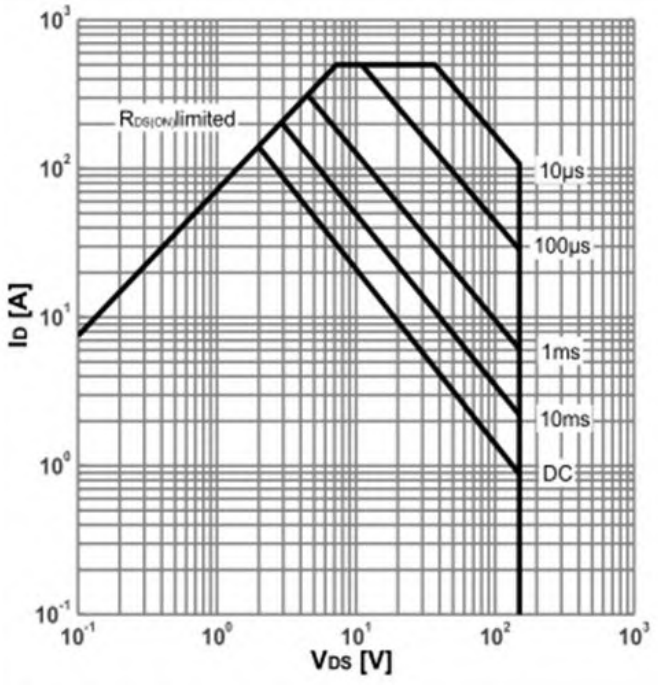
$P_{tot}=f(T_C)$

Diagram 2: Max. transient thermal impedance



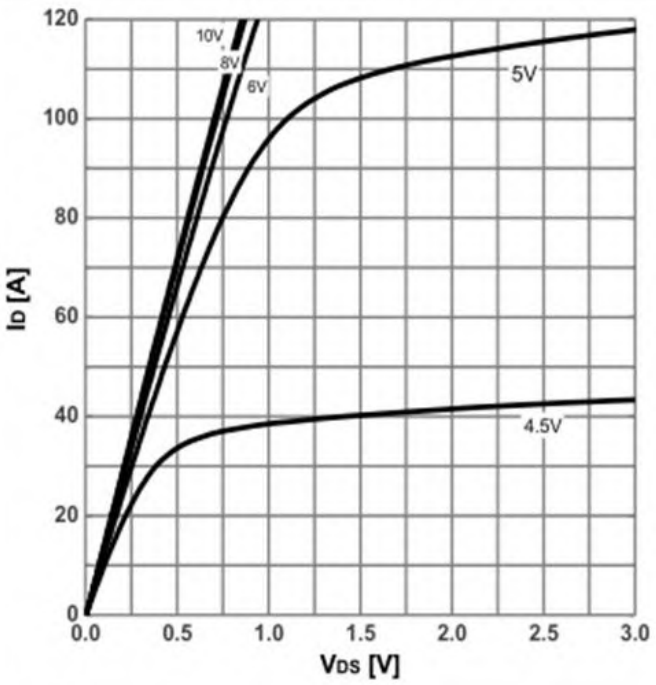
$Z_{thJC}=f(t_p)$; parameter: D= t_p/T

Diagram 3: Safe operating area



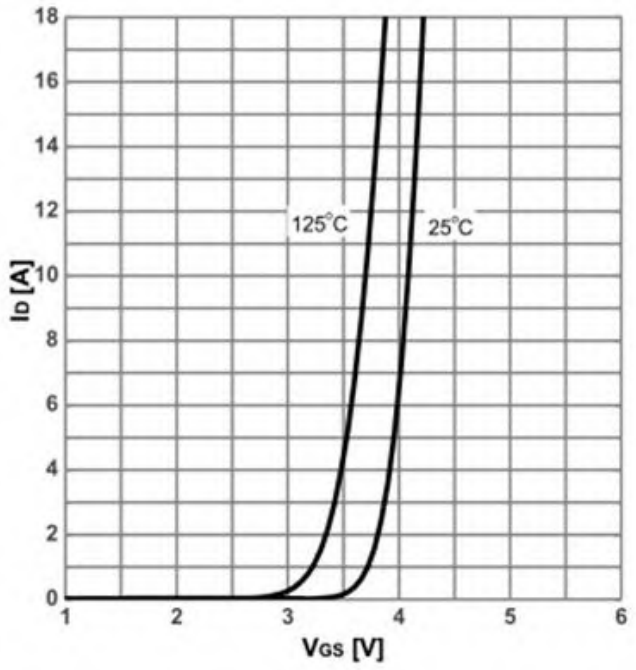
$I_D=f(V_{DS})$; T_j=25°C; D=0; parameter: t_p

Diagram 4: Typ. output characteristics



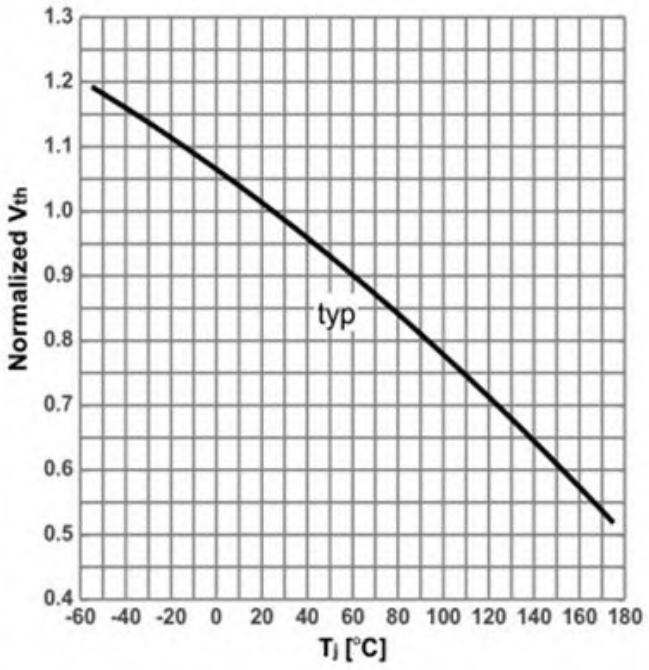
$I_D=f(V_{DS})$; T_j=25°C; parameter: V_{GS}

Diagram 5: Typ. transfer characteristics



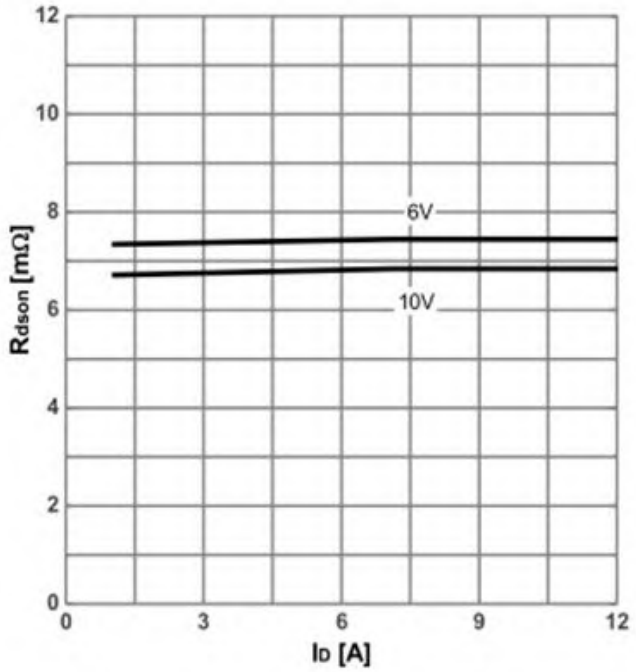
$I_D=f(V_{GS})$; V_{DS}=5V; parameter: T_j

Diagram 6: Gate threshold voltage vs. Junction temperature



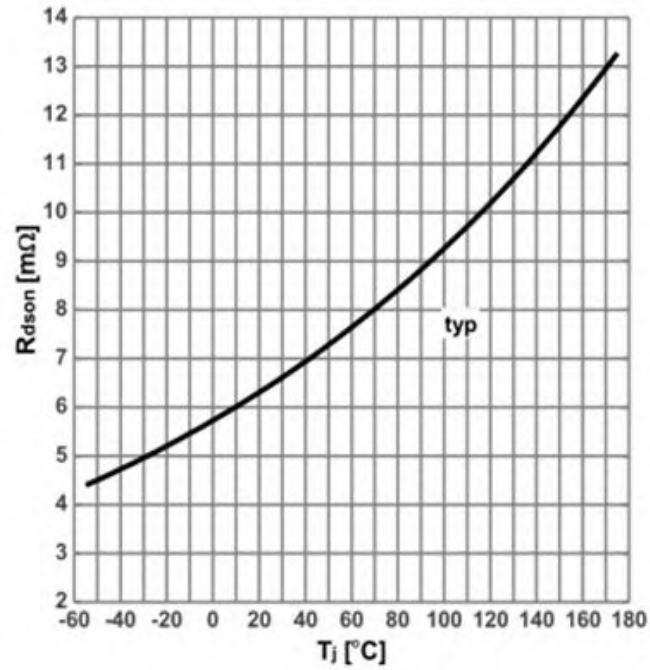
$V_{th}=f(T_j)$; I_D=250µA

Diagram 7: On-state resistance vs. Drain current



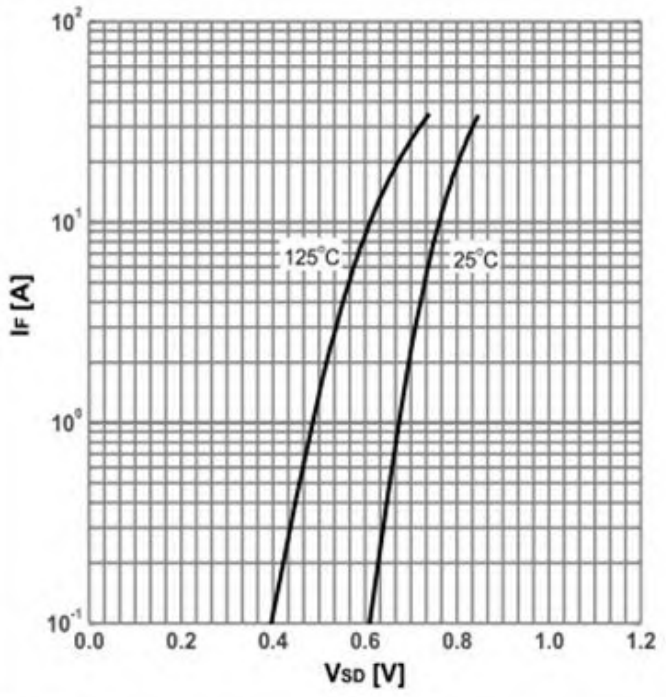
R_{DS}(on)=f(I_D); T_j=25°C; parameter: V_{GS}

Diagram 8: On-state resistance vs. Junction temperature



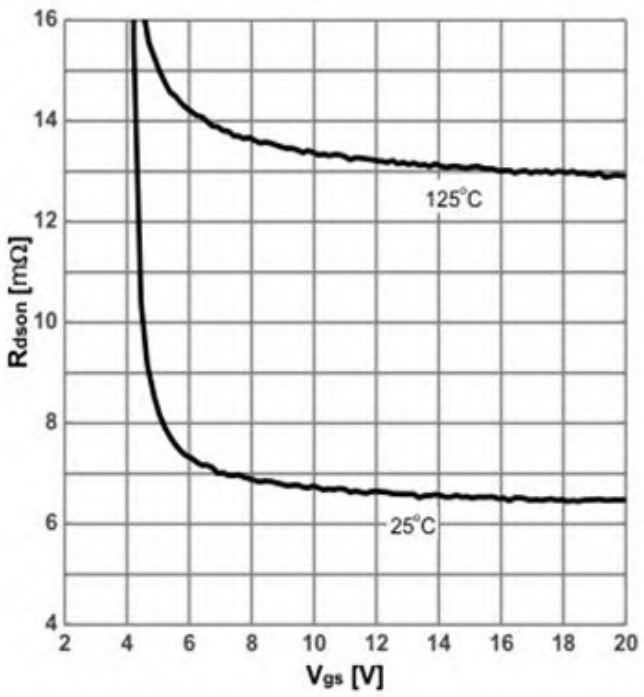
R_{DS}(on)=f(T_j); I_D=20A; V_{GS}=10V

Diagram 9: Forward characteristics of reverse diode



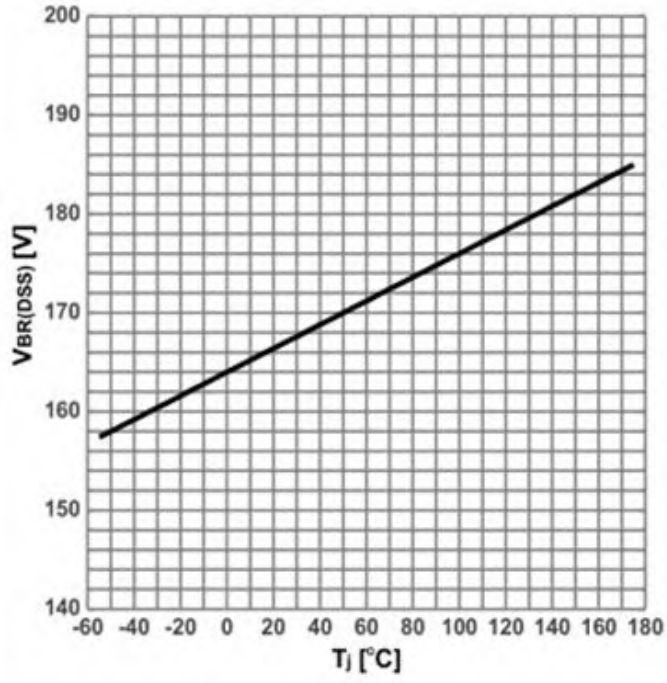
I_F=f(V_{SD}); parameter: T_j

Diagram 10: On-state resistance vs. Vgs characteristics



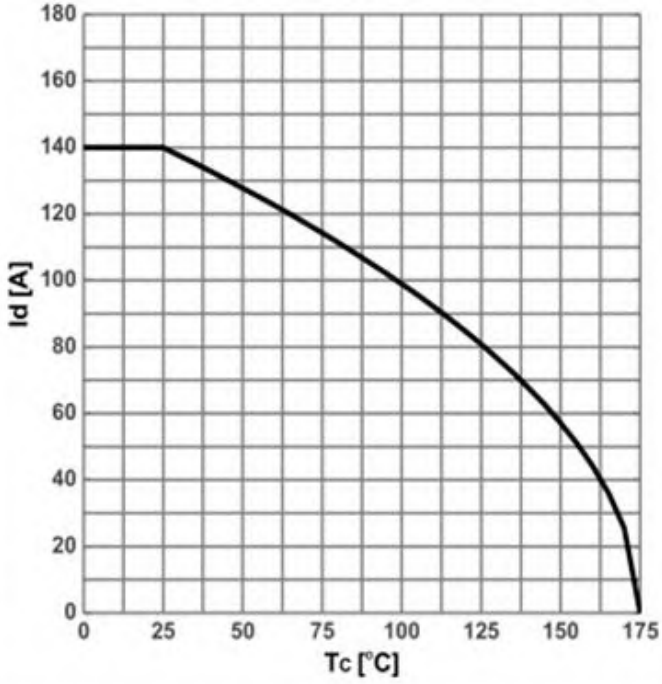
R_{DS}(on)=f(V_{gs}); I_D=20A; parameter: T_j

Diagram 11: Breakdown Voltage Variation vs. Temperature



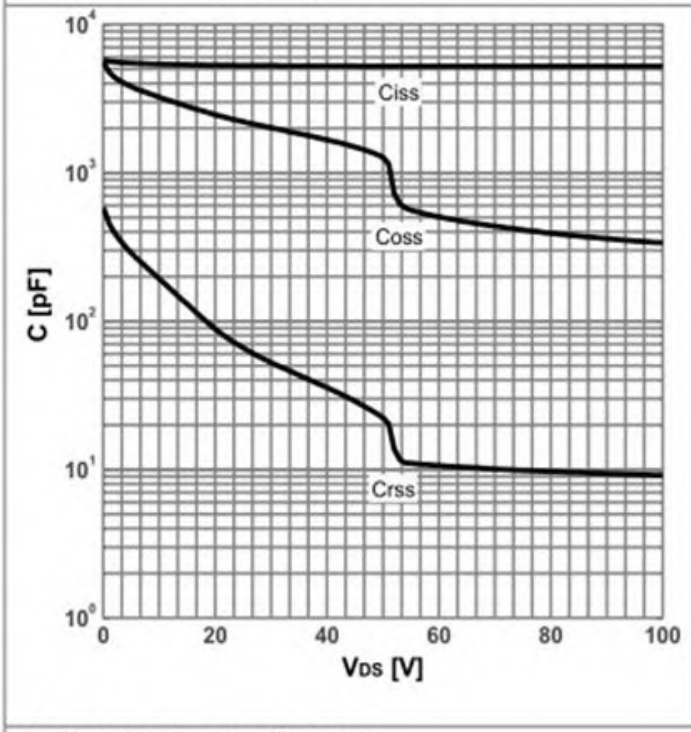
$V_{BR(DSS)}$=f(T_j); I_D=250μA

Diagram 12: Maximum Drain Current



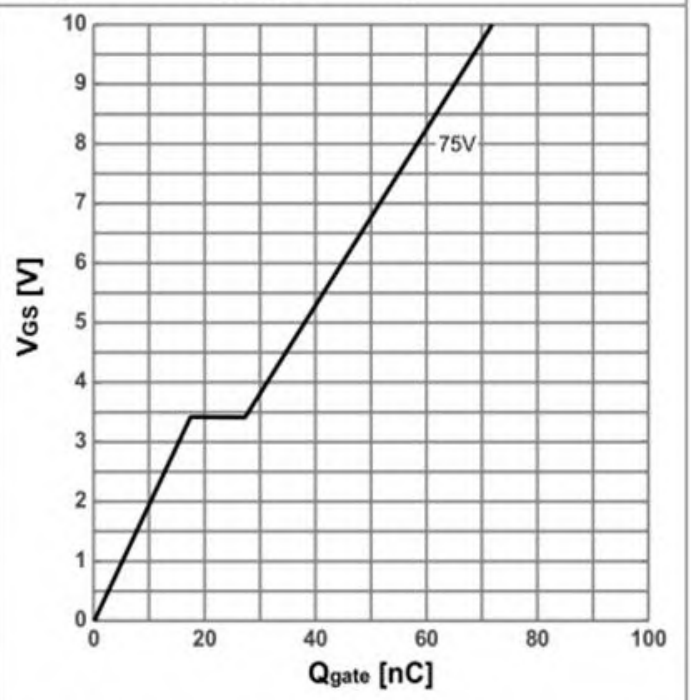
I_D= f(T_C); V_{GS}=10V

Diagram 13: Typ. capacitances



$C=f(V_{DS})$; $V_{GS}=0V$; f=1MHz

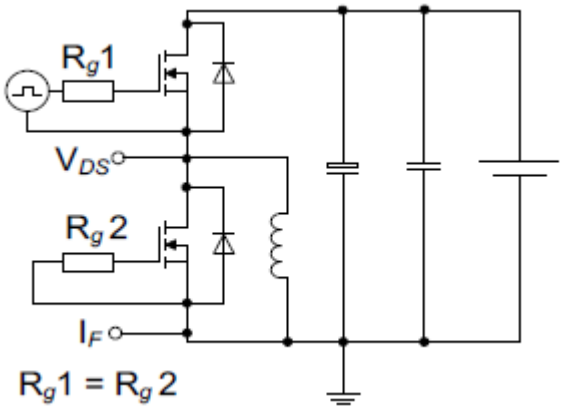
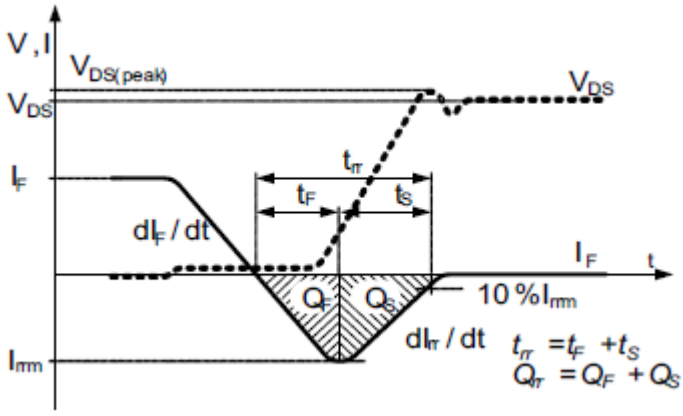
Diagram 14: Typ. gate charge



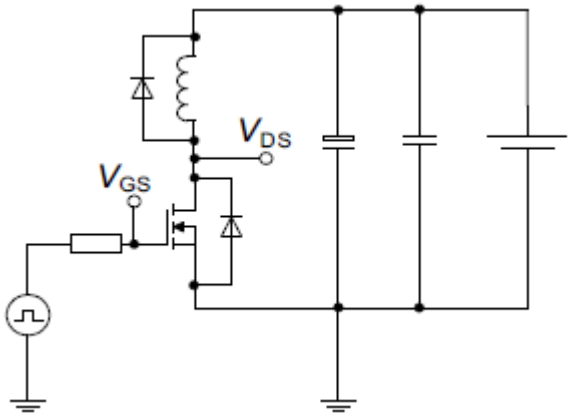
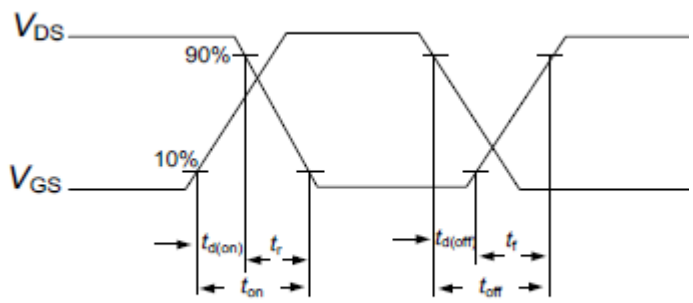
$V_{GS}=f(Q_{gate})$; $I_D=20A$ pulsed; $V_{DS}=75V$

Test Circuits

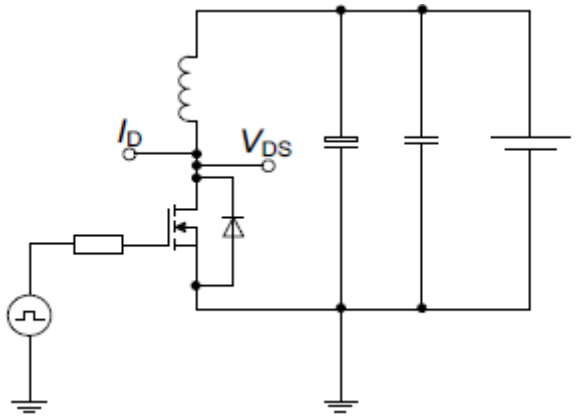
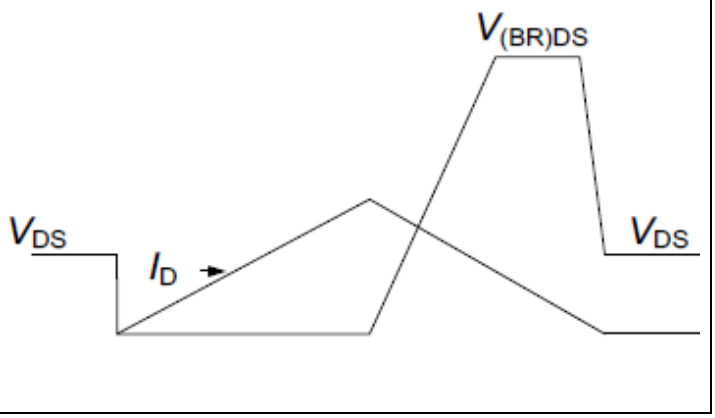
Diode Characteristics

Test circuit for diode characteristics	Diode recovery waveform
	

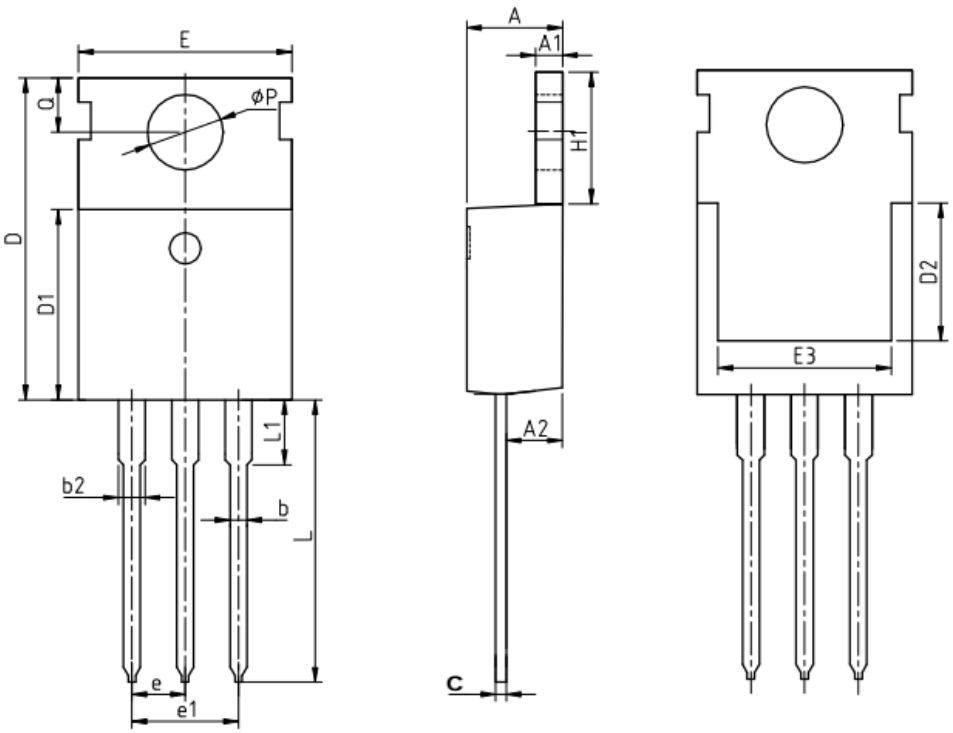
Switching Times

Switching times test circuit for inductive load	Switching times waveform
	

Unclamped Inductive Load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

Package Information ：TO-220



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	4.37	4.57	4.77
A1	1.15	1.30	1.45
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.17	1.27	1.47
c	0.40	0.50	0.65
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	-	-
E	9.70	10.00	10.30
E3	7.00	-	-
e	2.54 BSC		
e1	5.08 BSC		
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	-	3.10	3.40
ΦP	3.40	3.60	3.80
Q	2.60	2.80	3.00