

# FH1804GSB

## N-Channel Enhancement Mode Power MOSFET

### Description

The FH1804GSB uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

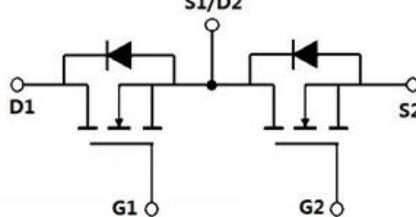
### Application

- Motor drivers
- Power switching application
- DC/DC Converters In Computing
- LCD TV appliances

### General Features

$V_{DS}=40V$  ;  $ID=60A / 80A$   
 $R_{DS(ON)}=4.0m\Omega$ (typ) @  $V_{GS}=10V$   
 $R_{DS(ON)}=5.7m\Omega$ (typ) @  $V_{GS}=4.5V$

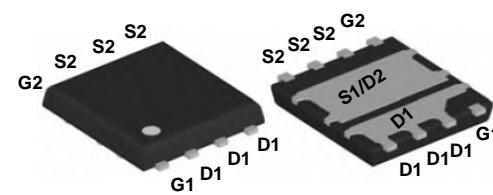
- High density cell design for ultra low  $R_{ds(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation



Schematic diagram



Marking and pin assignment



PDFN5x6-8L Pin assignment and Top / Bottom View

### Absolute Maximum Ratings

Symbol	Parameter	Channel 1	Channel 2	Unit
<b>Common Ratings</b> ( $T_c=25^\circ C$ Unless Otherwise Noted)				
$V_{DSS}$	Drain-Source Voltage	40	40	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	
$T_J$	Maximum Junction Temperature	150	150	$^\circ C$
$T_{STG}$	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$I_S$	Diode Continuous Forward Current	$T_c=25^\circ C$	30	A

### Mounted on Large Heat Sink

$I_{DM}^{①}$	300 $\mu$ s Pulsed Source Current	$T_c=25^\circ C$	120	160	A
$I_D^{②}$	Continuous Drain Current@ $T_c(V_{GS}=10V)$	$T_c=25^\circ C$	60	80	A
		$T_c=100^\circ C$	38	52	
$P_D$	Continuous Drain Current@ $T_a(V_{GS}=10V)^{③}$	$T_a=25^\circ C$	20	28	
		$T_a=70^\circ C$	16	22	
	Maximum Power Dissipation@ $T_c$	$T_c=25^\circ C$	30	42	W
		$T_c=100^\circ C$	12.5	17	
	Maximum Power Dissipation@ $T_a$	$T_a=25^\circ C$	4.2	4.2	
		$T_a=70^\circ C$	2.7	2.7	

Symbol	Parameter	Channel 1	Channel 2	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	4.7	3.9	°C/W
$R_{\theta JA}^{(3)}$	Thermal Resistance-Junction to Ambient	65	55	°C/W
$E_{AS}^{(4)}$	Avalanche Energy, Single Pulsed	100		mJ

**Electrical Characteristics** ( $T_C=25^\circ C$  Unless Otherwise Noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	40			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=40V, V_{GS}=0V$			1	$\mu A$
		$T_J=125^\circ C$			100	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1.0		2.5	V
$I_{GSS}$	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$			$\pm 100$	nA
$R_{DS(on)}^{(5)}$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=20A$		4.0	5.2	$m\Omega$
		$V_{GS}=4.5V, I_{DS}=15A$		5.7	7.6	$m\Omega$
<b>Diode Characteristics</b>						
$V_{SD}^{(5)}$	Diode Forward Voltage	$I_{SD}=20A, V_{GS}=0V$			1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD}=20A, dI_{SD}/dt=100A/\mu s$		20		ns
$Q_{rr}$	Reverse Recovery Charge			13		nC
<b>Dynamic Characteristics</b> <sup>(6)</sup>						
$R_G$	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1MHz$		1.4		$\Omega$
$C_{iss}$	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=20V,$ Frequency=1.0MHz		1105		$pF$
$C_{oss}$	Output Capacitance			246		
$C_{rss}$	Reverse Transfer Capacitance			31		
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=20V, R_L=1.00\Omega,$ $I_{DS}=20A, V_{GEN}=10V,$ $R_G=3\Omega$		9.2		$ns$
$t_r$	Turn-on Rise Time			23		
$t_{d(off)}$	Turn-off Delay Time			25.6		
$t_f$	Turn-off Fall Time			6		
<b>Gate Charge Characteristics</b> <sup>(6)</sup>						
$Q_g$	Total Gate Charge	$V_{DS}=20V, V_{GS}=10V,$ $I_{DS}=20A$		22.7		$nC$
$Q_{gs}$	Gate-Source Charge			3.84		
$Q_{gd}$	Gate-Drain Charge			4.8		

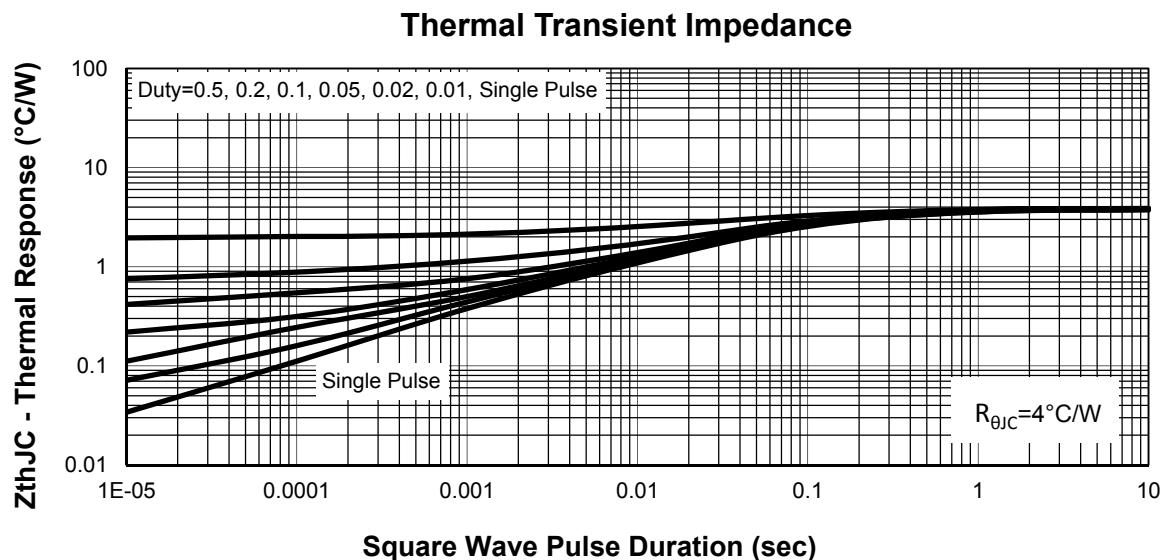
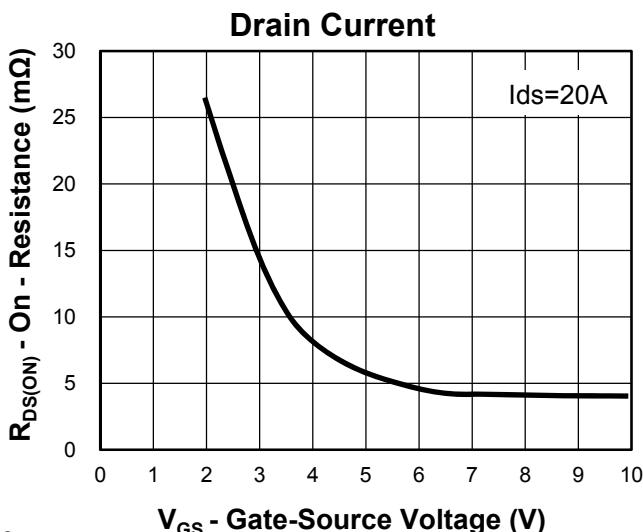
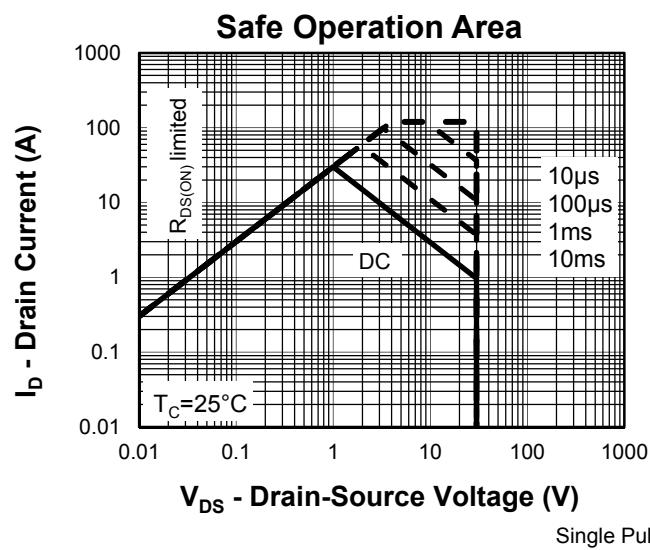
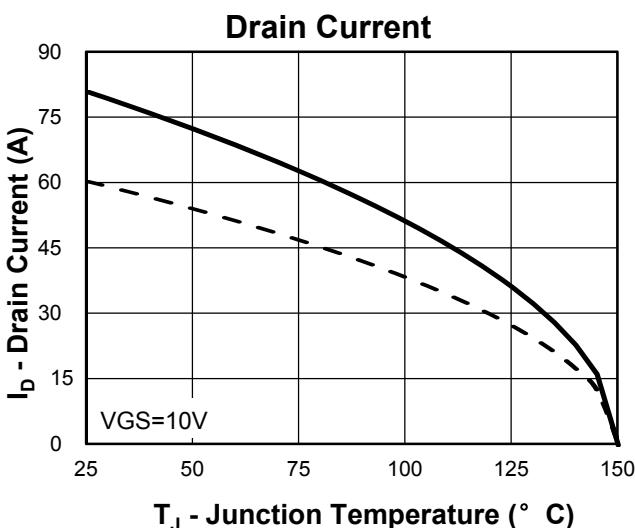
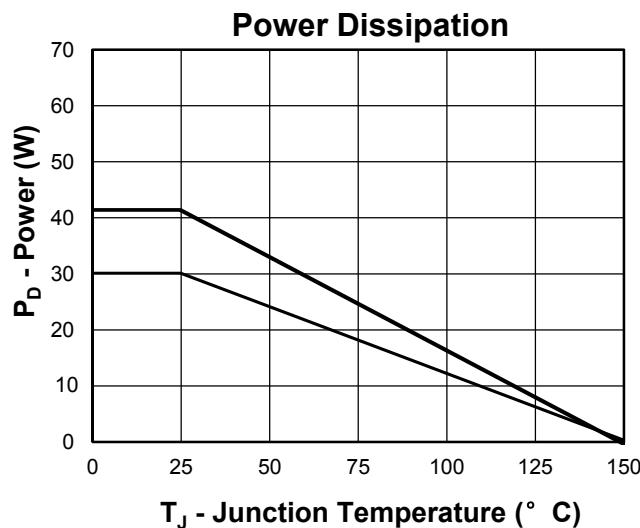
Notes: ①Pulse width limited by safe operating area.

②Calculated continuous current based on maximum allowable junction temperature.

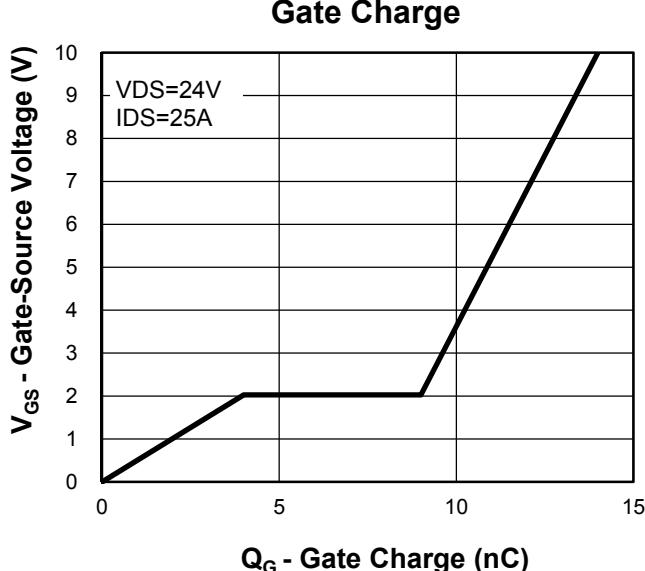
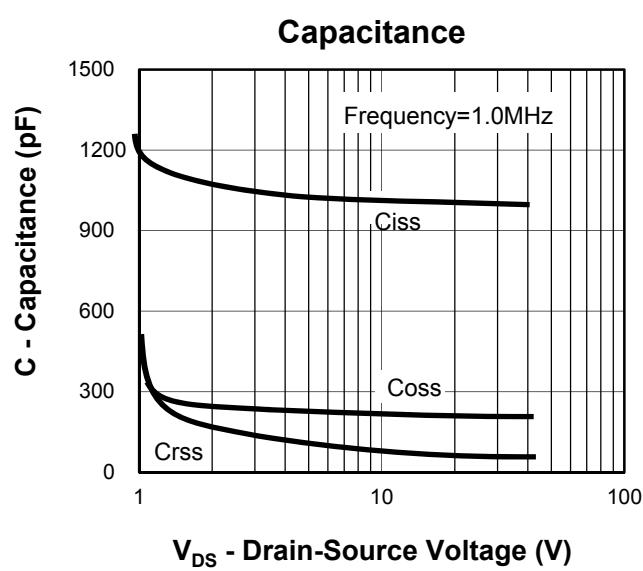
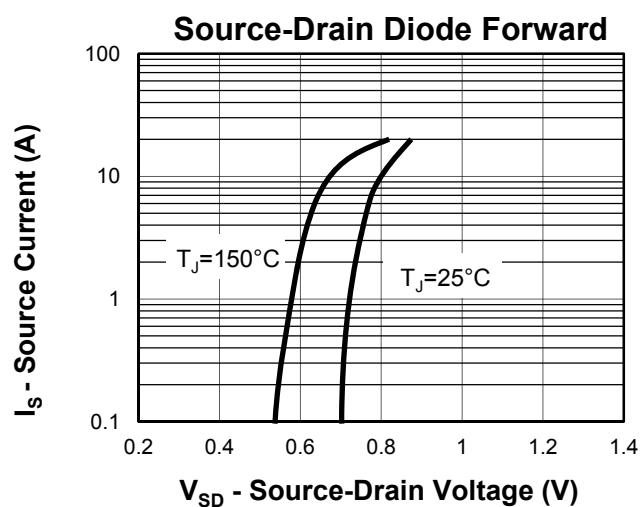
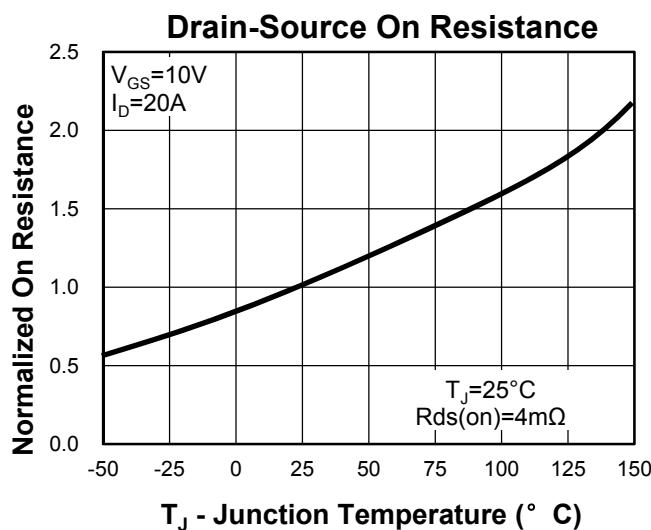
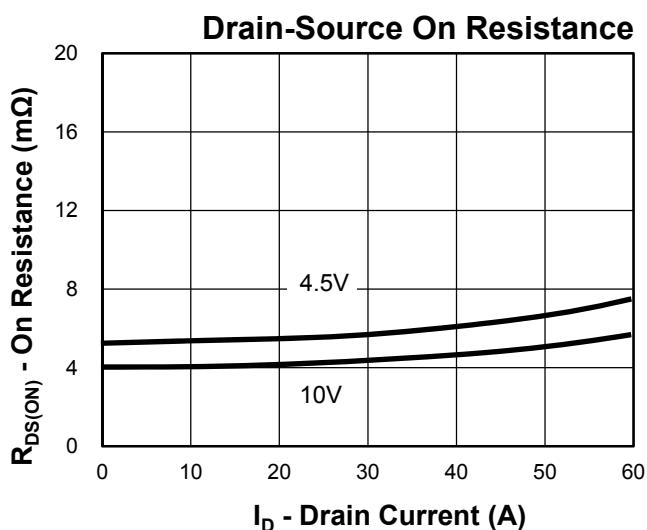
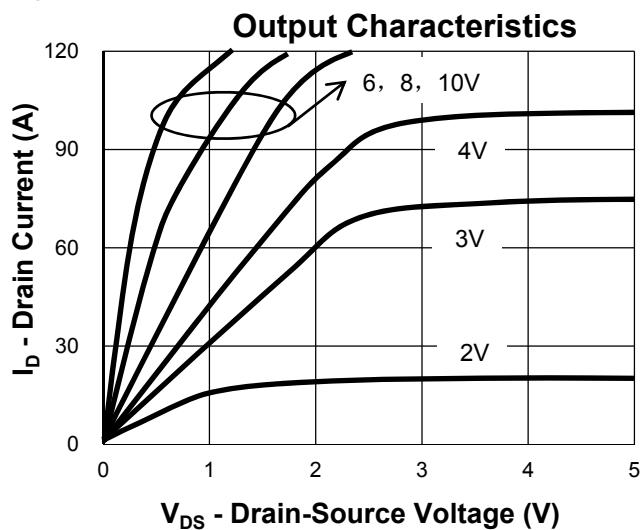
③When mounted on 1 inch square copper board,  $t \leq 10sec$ .④Limited by  $T_{Jmax}$ ,  $I_{AS} = 20A$ ,  $V_{DD} = 20V$ ,  $R_G = 50\Omega$ ,  $L = 0.5mH$ , Starting  $T_J = 25^\circ C$ .⑤Pulse test; Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .

⑥Guaranteed by design, not subject to production testing.

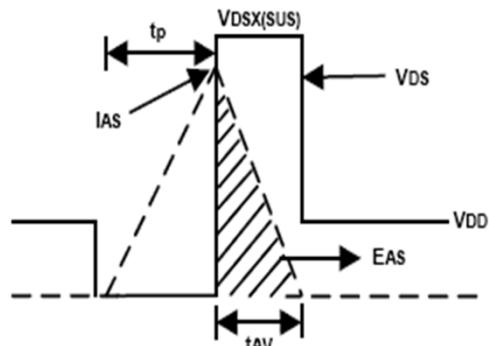
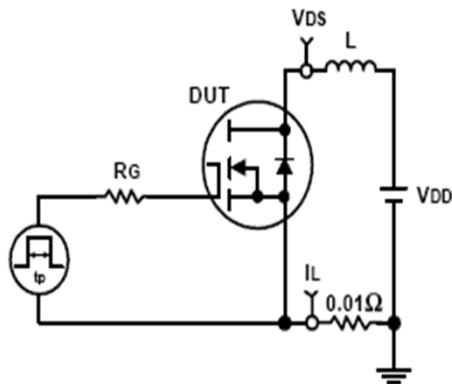
## Typical Characteristics



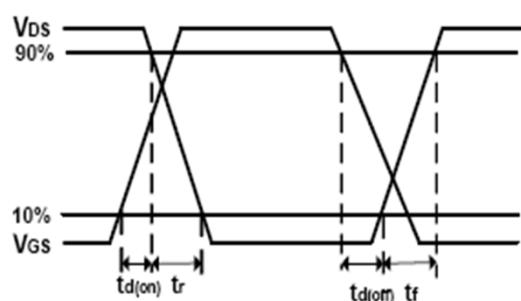
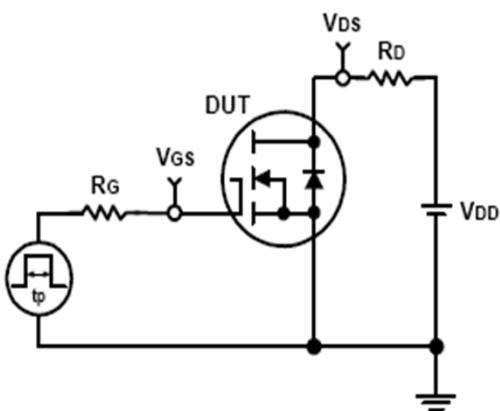
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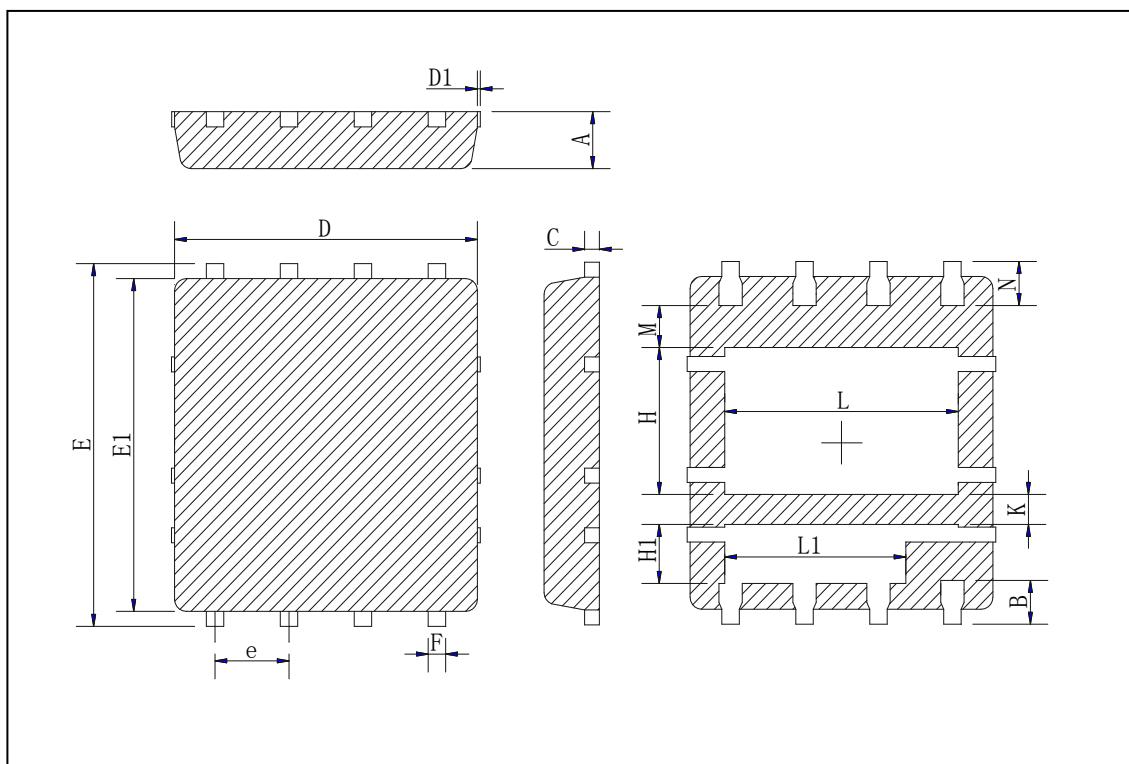


### Avalanche Test Circuit and Waveforms



### Switching Time Test Circuit and Waveforms



**Package Information : PDFN5x6-8L**

Symbol	Min	Typ	Max
A	0.90	0.95	1.00
B	0.60	0.70	0.80
C	0.20	0.254	0.30
D	5.10	5.20	5.30
D1			0.12
E	5.95	6.05	6.15
E1	5.40	5.55	5.70
e	1.22	1.27	1.32
F	0.25	0.30	0.35
H	2.35	2.45	2.55
H1	0.88	0.98	1.08
L	3.80	4.00	4.20
L1	3.00	3.10	3.20
M	0.60	0.70	0.80
N	0.63	0.73	0.83
K	0.40	0.50	0.60