

FH8609A2

One Cell Lithium-ion/Polymer Battery Protection IC

GENERAL DESCRIPTION

The FH8609A2 product is a high integrat ion solution for lithium-ion/polymer battery protection. FH8609A2 contains advanced power MOSFET, high-accuracy voltage de tection circuits and delay circuits. FH86 AJ is put into an ultra-small SOT23-5 pack age and only one external component mak es it an ideal solution in limited space of ba ttery pack.

FH8609A2 has all the protection function s required in the battery application includi ng overcharging, over-discharging, overcur rent and load short circuiting protection etc. The accurate overcharging detection voltag e ensures safe and full utilization charging. The low standby current drains little current from the cell while in storage.

The device is not only targeted for digital cellular phones, but also for any other Li-lo -n and Li-Poly battery-powered information appliances requiring long-term battery life.

FEATURES

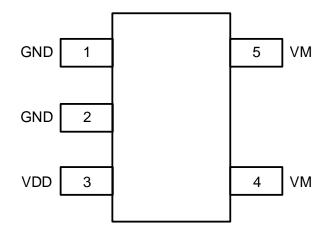
PIN CONFIGURATION

Protection of Charger Reverse Connection

- Protection of Battery Cell Reverse Con nection Without External Load
- Integrated Advanced Power MOSFET withEquivalentof 16.5 mΩRss(ON)
- Ultra-small SOT23-5 Package
- Only One External Capacitor Require
- Over-temperature Protection
- Overcharge Current Protection
- Two-step Overcurrent Detection
 -Overdischarge Current 1
 -Load Short Circuiting
- Low Current Consumption
 Operation Mode: 3.9µA typ
 Power-down Mode:2.2µA typ
- Charger Detection Function
- 0V Battery Charging Function
- Delay Times are generated inside
- High-accuracy Voltage Detection
- RoHS Compliant and Lead (Pb) Free

APPLICATIONS

One-Cell Lithium-ion Battery Pack Lithium-Polymer Battery Pack Power Bank



TOP View Figure 1. PIN Configuration

PIN DESCRIPTION

FH8609A2 PIN NUMBER	PIN NAME	PIN DESCRIPTION
1,2	GND	Ground, connect the negative terminal of the battery to this pin
3	VDD	Power Supply
4,5	VM	The negative terminal of the battery pack. The internal FET switch connects this terminal to GND

Typical Application

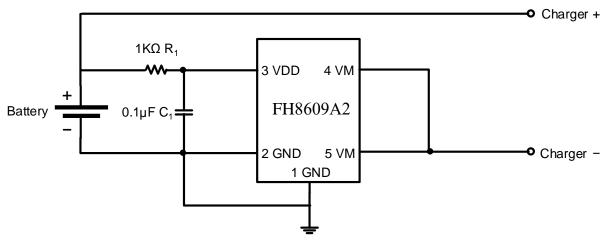


Figure 1. Basic Application Circuit

ABSOLUTE MAXIMUM RATINGS

(NOTE: DO NOT EXCEED THESE LIMITS TO PREVENT DAMAGE TO THE DEVICE. EXPOSURE TO ABSOLUTE MAXIMUM RATING CONDITIONS FOR LONG PERIODS MAY AFFECT DEVICE RELIABILITY.)

PARAMETER	VALUE	UNIT	
VDD input pin voltage	-0.3 to 6	V	
VM input pin voltage	-6 to 10	V	
Operating Ambient Temperature	-40 to 85	°C	
Maximum Junction Temperature	150	°C	
Storage Temperature	-55 to 150	°C	
Lead Temperature (Soldering, 10 sec)	300	°C	
Power Dissipation at T=25°C	0.4	W	
Package Thermal Resistance (Junction to Ambient) θJA	250	°C/W	
Package Thermal Resistance (Junction to Case) θJC	130	°C/W	
HBM ESD	2000	V	

ELECTRICAL CHARACTERISTICS

Typical and limits appearing in normal type apply for TA = 25°C, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
Detection Voltage						
Overcharge Detection Voltage	Vcu		4.25	4.30	4.35	V
Overcharge Release Voltage	Vcl		4.00	4.10	4.20	V
Overdischarge Detection Voltage	Vdl		2.3	2.4	2.5	V
Overdischarge Release Voltage	Vdr		2.9	3.0	3.1	V
Detection Current						
Overdischarge Current Detection	*liov1	VDD=3.6V	6	9	12	А
Overdischarge Current Recovery	*IROV1	VDD=3.6V	8.5	25	40	μA
Overcharge Current Detection	*Існос	VDD=3.6V	4	6	8	А
Load Short-Circuiting Detection	*ISHORT	VDD=3.6V	20	35	60	А
Current Consumption						
Current Consumption in Normal Opera- tion	IOPE	VDD=3.6V VM pin floating		3.9	6	μA
Current Consumption in Power Down	IPD	VDD=3.6V VM pin floating		2.2	4	μΑ
VM Internal Resistance						
Internal Resistance between VM and V	R∨mD	Vdd=3.6V Vm=1.0V	200	300	400	kΩ
Internal Resistance between VM and GND	R∨мs	VDD=3.6V VM pin floating	15	25	35	kΩ
FET on Resistance						
Equivalent FET on Resistance	*Rss(on)	VDD=3.6V IVM=1.0A		16.5	25	mΩ
Over Temperature Protection						
Over Temperature Protection	*TSHD+			150		°C
Over Temperature Recovery Degree	*Tshd-			110		°C
Detection Delay Time						
Overcharge Voltage Detection Delay- Time	tcu		80	130	180	mS
Overdischarge Voltage Detection Delay Time	tDL		20	40	60	mS
Overdischarge Current1 Detection De- lay Time	tiov1	VDD=3.6V	4	8	18	mS
Overcharge Current Detection Delay Time	*tснос	VDD=3.6V	5	10	20	mS
Load Short-Circuiting Detection De- lay Time	*tshort	Vdd=3.6V	50	300	600	μS

Note1: * The parameter is guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM

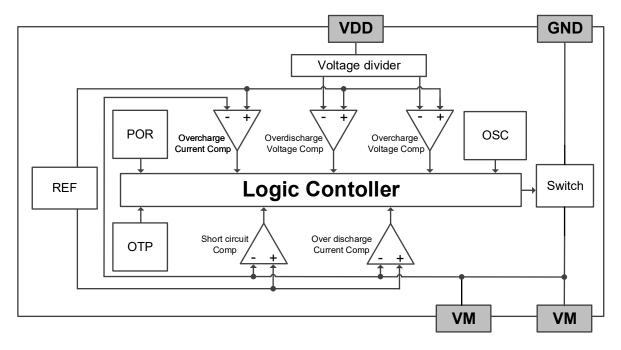


Figure 3. Functional Block Diagram

FUNCTIONAL DESCRIPTION

The FH8609A2 monitors the voltage and current of a battery and protects it from being damaged due to overcharge voltage, overdischarge voltage, overdischarge current, and short circuit conditions by disconnecting the battery from the load or charger. The se functions are required in order to operate the battery cell within specified limits. The device requires only one external capacito r. The MOSFET is integrated and its R ss(o N) is as low as 16.5m Ω typical.

Normal Mode

If no exception condition is detected, ch arging and discharging can be carried out freely. This condition is called the normal o perating mode.

Overcharge Condition

When the battery voltage becomes highe r than the overcharge detection voltage (V CU) during charging under normal conditio n and the state continues for the overcharg e detection delay time (t_{CU}) or longer, the FH8609A2 turns the charging control FET off to stop charging. This condition is called th e overcharge condition. The overcharge co ndition is released in the following two case s:

1. When the battery voltage drops below the overcharge release voltage (V_{CL}), the F H8609A2 turns the charging control FET on and returns to the normal condition.

2. When a load is connected and dischar ging starts, the FH8609A2 turns the chargi ng control FET on and returns to the norma l condition. The release mechanism is as fo llows: the discharging current flows through an internal parasitic diode of the charging F ET immediately after a load is connected a nd discharging starts, and the VM pin volta ge increases about 0.7 V (forward voltage of the diode) from the GND pin voltage mo mentarily. The FH8609A2 detects this volta ge and releases the overcharge condition. Consequently, in the case that the battery voltage is equal to or lower than the overch arge detection voltage (V_{CU}), the FH8609A2 returns to the normal condition immediatel y, but in the case the battery voltage is hig her than the overcharge detection voltage (V_{CU}),the chip does not return to the normal condition until the battery voltage drops bel ow the overcharge detection voltage (V_{CU}) even if the load is connected. In addition, if the VM pin voltage is equal to or lower than the overcurrent 1 detection voltage when a load is connected and discharging starts, t he chip does not return to the normal condi tion.

Remark

If the battery is charged to a voltage higher than t he overcharge detection voltage (Vcu) and the batte ry voltage does not drops below the overcharge det ection voltage (Vcu) even when a heavy load, which causes an overcurrent, is connected, the overcurre nt 1 and overcurrent 2 do not work until the battery voltage drops below the overcharge detection volta ge (Vcu). Since an actual battery has, however, an i nternal impedance of several dozens of m Ω , and th e battery voltage drops immediately after a heavy lo ad which causes an overcurrent 2 work. Detection of I oad short-circuiting works regardless of the battery voltage.

Overdischarge Condition

When the battery voltage drops below th e overdischarge detection voltage (VDL) duri ng discharging under normal condition and it continues for the overdischarge detection delay time (t_{DL}) or longer, the FH8609A2 tur ns the discharging control FET off and stop s discharging. This condition is called over discharge condition. After the discharging c ontrol FET is turned off, the VM pin is pulle d up by the R_{VMD} resistor between VM and V DD in FH8609A2. Meanwhile when VM is b igger than 1.5V (typ.) (the load short-circuiti ng detection voltage), the current of the ch ip is reduced to the power-down current (IPD N). This condition is called power-down con dition. The VM and VDD pins are shorted b y the RVMD resistor in the IC under the overd ischarge and power-down conditions.

The power-down condition is released w hen a charger is connected and the potenti al difference between VM and VDD becom es 1.3 V (typ.) or higher (load short-circuitin g detection voltage). At this time, the FET i s still off. When the battery voltage become s the overdischarge detection voltage(VDL) or higher (see note), the FH8609A2 turns t he FET on and changes to the normal con dition from the overdischarge condition.

Remark

If the VM pin voltage is no less than the charger d etection voltage (V_{CHA}), when the battery under over discharge condition is connected to a charger, the o verdischarge condition is released (the discharging control FET is turned on) as usual, provided that the battery voltage reaches the overdischarge release v oltage (V_{DU}) or higher.

Overcurrent Condition

When the discharging current becomes equal to or higher than a specified value (th e VM pin voltage is equal to or higher than the overcurrent detection voltage) during di scharging under normal condition and the s tate continues for the overcurrent detection delay time or longer, the FH8609A2 turns o ff the discharging control FET to stop disch arging. This condition is called overcurrent condition. (The overcurrent includes overcu rrent, or load short-circuiting.)

The VM and GND pins are shorted intern ally by the R_{VMS} resistor under the overcurre nt condition. When a load is connected, the VM pin voltage equals the VDD voltage du e to the load.

The overcurrent condition returns to the normal condition when the load is released and the impedance between the B+ and B-pins becomes higher than the automatic re coverable impedance. When the load is re moved, the VM pin goes back to the GND potential since the VM pin is shorted the G ND pin with the Rvms resistor. Detecting that the VM pin potential is lower than the overc urrent detection voltage (Viov), the IC return s to the normal condition.

Abnormal Charge Current Detection

If the VM pin voltage drops below the ch arger detection voltage (V_{CHA}) during chargi ng under the normal condition and it contin ues for the overcharge detection delay time (t_{CU}) or longer, the FH8609A2 turns the cha rging control FET off and stops charging. T his action is called abnormal charge curren t detection.

Abnormal charge current detection work s when the discharging control FET is on a nd the VM pin voltage drops below the cha rger detection voltage (V_{CHA}). When an abn ormal charge current flows into a battery in the overdischarge condition, the FH8609A2 consequently turns the charging control FE T off and stops charging after the battery v oltage becomes the overdischarge detectio n voltage and the overcharge detection del ay time (t_{cu}) elapses.

Abnormal charge current detection is rel eased when the voltage difference betwee n VM pin and GND pin becomes lower tha n the charger detection voltage (V_{CHA}) by se parating the charger. Since the 0 V battery charging function has higher priority than th e abnormal charge current detection functi on, abnormal charge current may not be de tected by the product with the 0 V battery c harging function while the battery voltage is low.

Load Short-circuiting condition

If voltage of VM pin is equal or below sho rt circuiting protection voltage (V_{SHORT}), the FH8609A2 will stop discharging and battery is disconnected from load. The maximum d elay time to switch current off is t_{SHORT}. This status is released when voltage of VM pin i s higher than short protection voltage ($V_{SH ORT}$), such as when disconnecting the load.

Delay Circuits

The detection delay time for overdischarg e current 2 and load short-circuiting starts when overdischarge current 1 is detected. As soon as overdischarge current 2 or load short-circuiting is detected over detection d elay time for overdischarge current 2 or loa d short-circuiting, the FH8609A2 stops disc harging. When battery voltage falls below o verdischarge detection voltage due to over discharge current, the FH8609A2 stop disc harging by overdischarge current detection. In this case the recovery of battery voltage i s so slow that if battery voltage after overdi scharge voltage detection delay time is still lower than overdischarge detection voltag e, the FH8609A2 shifts to power-down.

0V Battery Charging Function (1) (2) (3)

This function enables the charging of a connected battery whose voltage is 0V by self-discharge. When a charger having 0V battery start charging charger voltage (V_{OCHA}) or higher is connected between B+ and B- pins, the charging control FET gate is fixed to VDD potential. When the voltage between the gate and the source of the charging control FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging control FET is turned on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. If the battery voltage becomes equal to or higher than the overdischarge release voltage (V_{DU}), the normal condition returns.

Note:

(1) Some battery providers do not recommend charging of completely discharged batteries. Please refer to battery providers before the selection of 0 V battery charging function.

(2) The 0V battery charging function has higher priority than the abnormal charge current detection function. Consequently, a product with the 0 V battery charging function charges a battery and abnormal charge current cannot be detected during the battery voltage is low (at most 1.8 V or lower).

(3) When a battery is connected to the IC for the first time, the IC may not enter the normal condit ion in which discharging is possible. In this case, s et the VM pin voltage equal to the GND voltage (s hort the VM and GND pins or connect a charger) to enter the normal condition.

TIMING CHART

Vcu VCU-VHC Battery voltage VDL+VDH Vdl ٥N Internal Drive Signal OFF Vdd VM Vov1 Vss VCH4 Charger connection Load connection tcu (2) (1) (1) (3) (1)

1. Overcharge and Overdischarge voltage detection



Remark: (1) Normal condition (2) Overcharge voltage condition (3) Overdischarge voltage condition

2. Overdischarge Current and Load Short detection

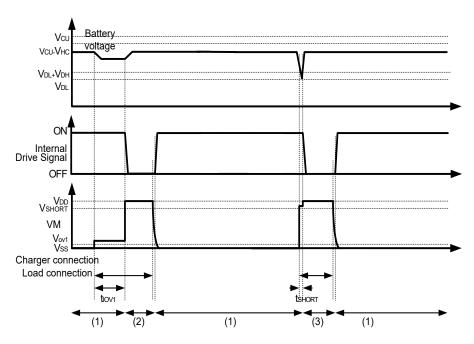


Figure 4-2 Overdischarge Current and Short Detection

Remark: (1) Normal condition (2) Overcharge voltage condition (3) Overdischarge voltage condition

3. Abnormal Charger Detection

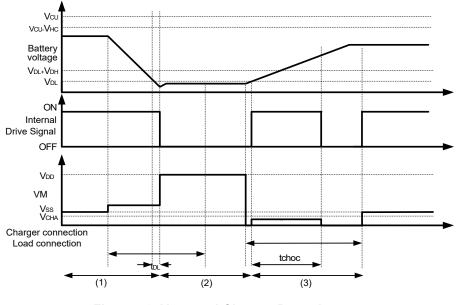


Figure4-3 Abnormal Charger Detection

Remark: (1) Normal condition (2) Overdischarge voltage condition (3) Overcharge voltage condition

TYPICAL APPLICATION

As shown in Figure 5, the current path and must be kept as short & heavy as possibl e. C1 is a filter decoupling circuit and should be as close as possible to VCC pin of FH8609A2.

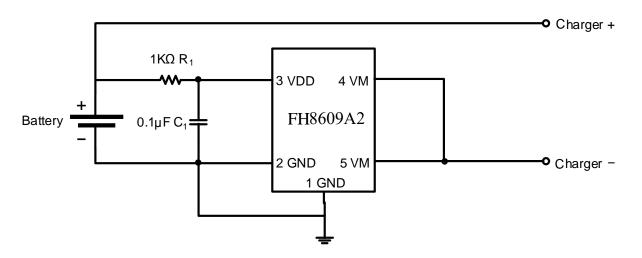


Figure 5 FH8609A2 in a Typical Battery Protection Circuit

Symbol	Тур	Value range	Unit
C1	0.1	0.1~2.2	μF
R1	1	0.47~2	KΩ

Remark:

1. The above parameters may be changed without notice;

2. The schematic diagram and parameters of the IC are not used as the basis to ensure the operation of the circuit. Please conduct full measurement on the actual application circuit before setting the parameters.

Precautions

• Pay attention to the operating conditions for input/output voltage and load current so that the power loss in FH8609A2 does not exceed the power dissipation of the package.

• Do not apply an electrostatic discharge to this FH8609A2 that exceeds the performance ratings of the built-in electrostatic protection circuit.

APPLIED MEASUREMENT METHOD

(1).Overcharge characteristic test method:

a. According to the figure6-1, connect the power supply DC1 to the B + and GND pins of the syste m board and set the voltage to about 3.6V. Connect the power supply from GND to VM to DC2 power sup ply and set 100mV current limiting 10mA. Observe the waveform.

b. Adjust the power supply voltage V1 and increase it by 0.001V until the output level of VM pin chang es from 0 to negative (-100mV). Record the overcharge protection voltage and measure the protection d elay.

c. Adjust the power supply voltage V1 to decrease by 0.001V until the output voltage of VM pin is recovered from negative (-100mV) to 0 level, and record the overcharge recovery voltage.

(2).Over discharge characteristic test method:

a. According to the figure6-2, connect the power supply DC1 to the B + and GND pins of the syste m board and set the voltage to about 3.6V. Connect the DC2 power supply from VM to GND, set the 100m V current limiting 10mA, and observe the waveform.

b. Adjust the power supply voltage V1 and increase it by 0.001V until the output level of VM pin chang es from 0 to positive (100mV). Record the overcharge protection voltage and measure the protection d elay.

c. Adjust the power supply voltage V1 to decrease by 0.001 V until the output voltage of VM pin is re stored from positive (100 mV) to 0 level, and record the overcharge recovery voltage.

(3).Discharge over current test method:

a. According to the figure 6-3, connect the DC1 power supply to the B + and GND pins of the syste m board and set the voltage to about 3.0V/3.6V/4.2V. Connect the electronic load from B + to VM and ob serve the waveform.

b. Adjust the electronic load increase it by 0.1A step, detect that the current from B + to VM is d off and meet the delay standard (about 10ms), and record the discharge delay time.

(4).Charging over current test method:

a. According to the figure6-4, connect the DC1 power supply to the B + and GND pins of the syste m board and set the voltage to about 3.0V/3.6V/4.2V, and load DC2 power supply from GND to VM.

b. Adjust the current limiting value of DC2 power supply to increase by 0.1A step, detect that the curre nt from GND to VM is turned off and meet the delay standard(about 10ms), and record the charging o ver-current delay time.

(5).lq test method:

a. As shown in the figure6-5, connect the positive pole of DC1 to B +, and the negative pole to GND, and set the voltage to 3.6V;

b. VM grounding, record the current passing through DC1 (Iq).

(6).Isd test method:

a. As shown in the figure6-6, connect the positive pole of DC1 to B + and the negative pole to GND, and set the voltage to 2V;

b. VM is suspended and the current passing through DC1 is recorded as Isd.

SCHEMATIC DIAGRAM OF TEST METHOD

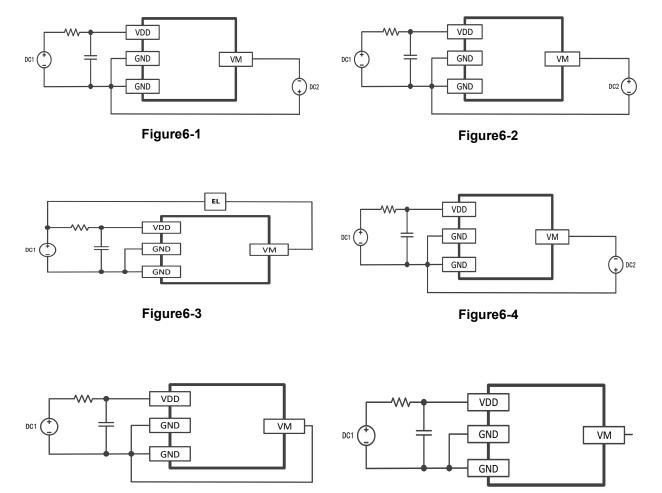
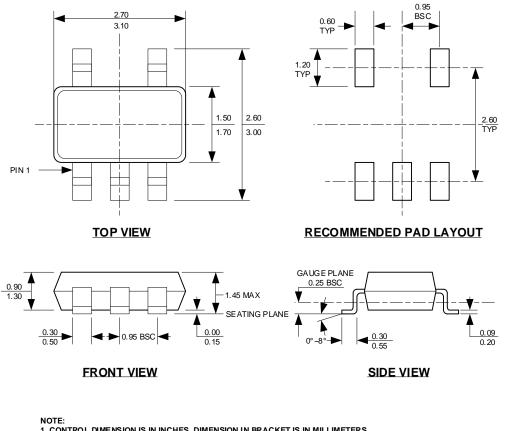


Figure6-5

Figure6-6

Package Information: SOT23-5



1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.

- CONTINUE DIMENSION IN INTROPES. DIMENSION IN BRACKET IS IN MILLIMETERS.
 PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
 LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
 DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6. DRAWING IS NOT TO SCALE.

NOTICE:

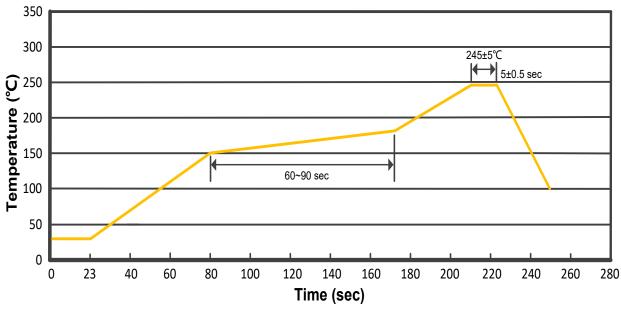
1. The information here contained could be changed without notice owing to product and/or technical

improvements. Please make sure before using the product that the information you are referring to is up to date.

2. No responsibilities are assumed by us for any consequence resulting from any wrong or improper operation, etc. of

the product

Solderability Curve of Lead-Free Reflow Soldering (applicable to SMT tube)



IR REFLOW PROFILE

Explain:

- 1.Preheating temperature 25~150°C, duration 60~90sec;
- 2.Peak temperature $245 \pm 5 \,^{\circ}$ C, duration 5 ± 0.5 sec;

3.Cooling rate of welding process is 2~10°C/sec.

Resistance to welding heat conditions

Temperature: 270±5°C; Time:10±1sec