

**FH2050DC****N-Channel Trench Power MOSFET****◆ General Description**

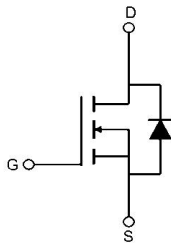
The FH2050DC is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

◆ Features

- $R_{DS(ON)} \leq 265 \text{ m}\Omega @ V_{GS}=10\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

◆ Applications

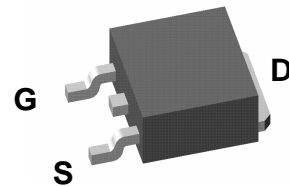
- DC/DC Converter
- Load Switch
- LCD/ LED Display inverter



Schematic diagram

TO-252

Marking and pin assignment



TO-252 top view

Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		250	V
V_{GSS}	Gate-Source Voltage		± 25	V
I_D	Continuous Drain Current ^{note5}	$T_C = 25^\circ\text{C}$	15	A
I_D	Continuous Drain Current ^{note5}	$T_C = 100^\circ\text{C}$	10	A
I_{DM}	Pulsed Drain Current ^{note3}		60	A
P_D	Power Dissipation ^{note2}	$T_C = 25^\circ\text{C}$	35	W
I_{AS}	Avalanche Current ^{note3,6}		5	A
E_{AS}	Single Pulse Avalanche Energy ^{note3,6}		125	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ^{note1,4}		62.5	$^\circ\text{C/W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$

◆ **Electrical Characteristics** ($T_J=25^{\circ}\text{C}$, unless otherwise n Specified)

Static

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	250	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
I_{GSS}	Gate Body Leakage	$V_{DS}=0V, V_{GS}=\pm 25V$	-	-	± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=200V, V_{GS}=0V$	-	-	1	μA
$R_{DS(ON)}$	Drain-Source On On-Resistance	$V_{GS}=10V, I_D=7A$	-	220	265	m Ω
V_{SD}	Diode Forward Voltage	$I_S=1A, V_{GS}=0V$	-	0.74	1	V

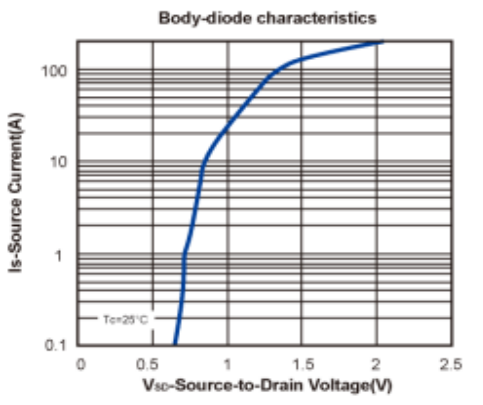
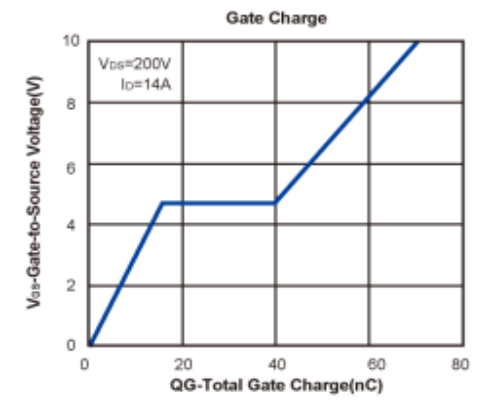
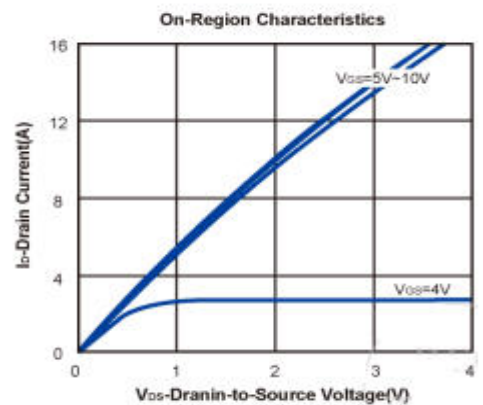
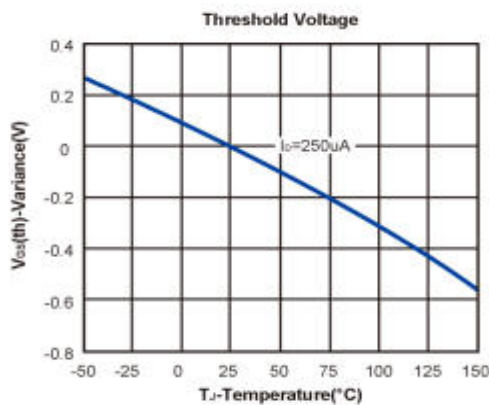
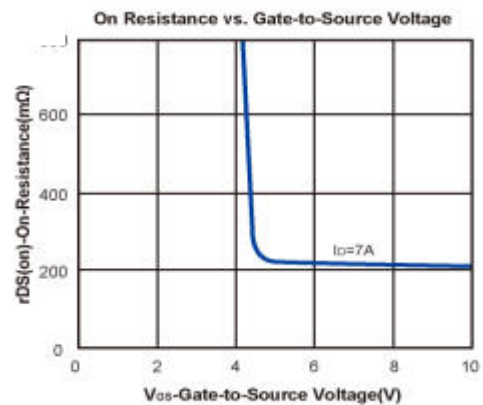
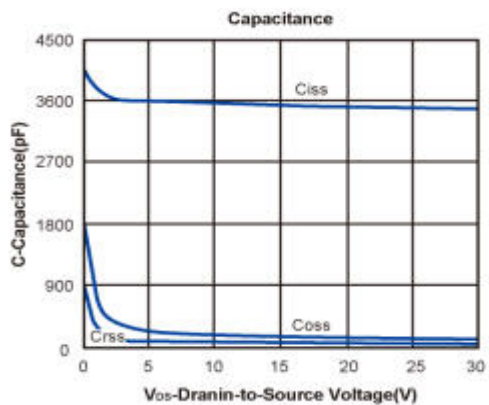
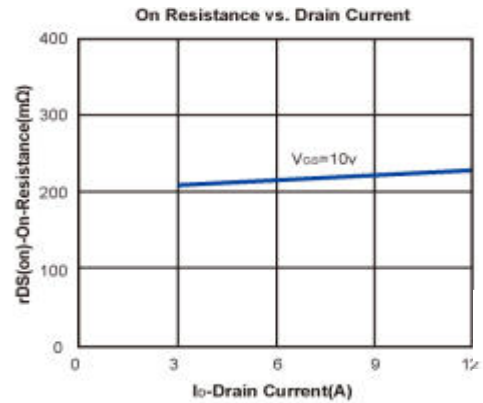
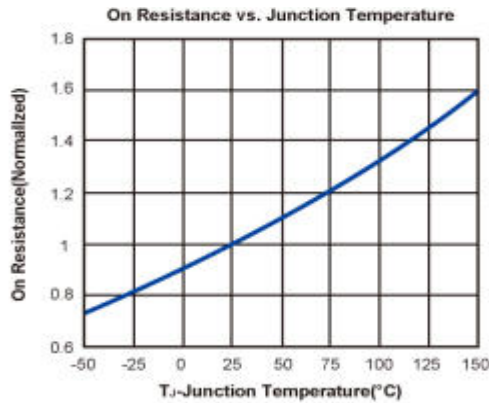
Dynamic

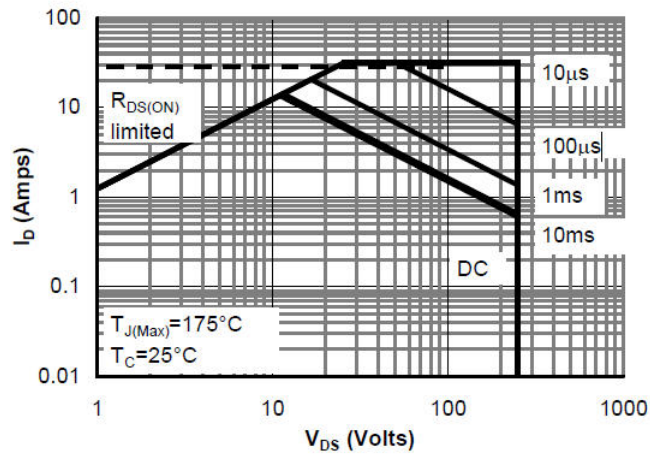
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Q_g	Total Gate Charge	$V_{DD}=200V$	-	70.8	-	nC
Q_{gs}	Gate-Source Charge	$V_{GS}=10V$	-	16.2	-	
Q_{gd}	Gate-Drain Charge	$I_D=14A$	-	23.9	-	
C_{iss}	Input Capacitance	$V_{DS}=25V$	-	3480	-	pF
C_{oss}	Output Capacitance	$V_{GS}=0V$	-	112	-	
C_{riss}	Reverse Transfer Capacitance	$f=1MHz$	-	51	-	
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=125V$	-	53	-	ns
t_r	Turn-On Rise Tim Time	$V_{GS}=10V$	-	62.6	-	
$t_{d(off)}$	Turn-Off Delay Time	$R_L=18\Omega$	-	198	-	
t_f	Turn-Off Fall Time	$R_G=25\Omega$ $I_D=7A$	-	83.5	-	

Notes:

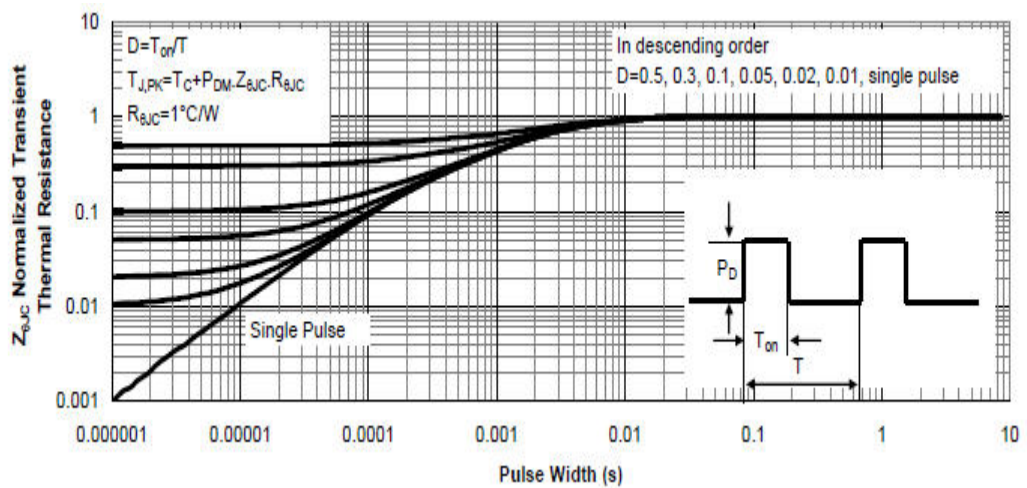
1. The value of $R_{\theta JC}$ is measured in a still air environment with $T_A=25^{\circ}\text{C}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.
2. The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
3. Single pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$.
4. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
5. The maximum current rating is package limited.
6. The EAS data shows Max. rating. The test condition is $V_{DS}=150V, V_{GS}=10V, L=10mH$

◆ Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)



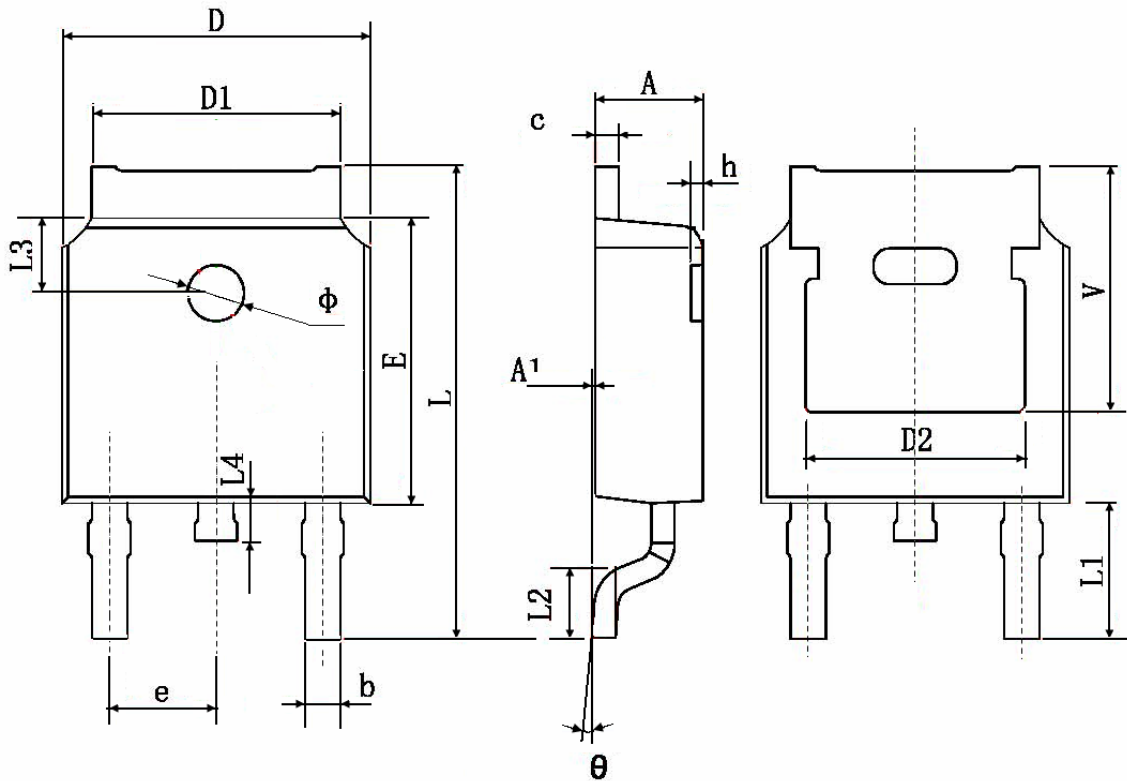


Maximum Forward Biased Safe Operating Area



Normalized Maximum Transient Thermal Impedance

Package Information : TO-252



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	