FH3090G

N-Channel Trench Power MOSFET

Description

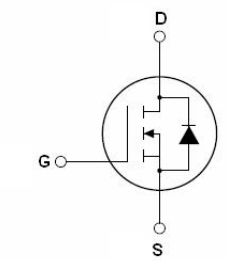
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on state resistance, provide superior switching performance, and with stand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

General Features

- V_{DSS}=30V , ID=85A
  $R_{DS(ON)}$ =3.7mΩ (Typ) @V_{GS}=10V
  $R_{DS(ON)}$ =5.9mΩ (Typ) @V_{GS}=4.5V
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green device available

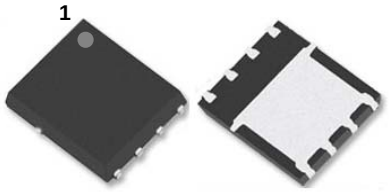
Applications

- Motor Drives
- UPS
- DC-DC Converter



Schematic diagram

Marking and pin Assignment



PDFN5X6-8L top and bottom view

Absolute Maximum Ratings (T_C=25℃ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current	T_C = 25℃	85	A
		T_C = 100℃	52	A
I_{DM}	Pulsed Drain Current note1		240	A
E_{AS}	Single Pulsed Avalanche Energy note2		270	mJ
P_D	Power Dissipation	T_C = 25℃	55	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2.27	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics (T_C=25℃ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =30V, V_{GS} = 0V,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS} =0V,V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance note3	V_{GS} =10V, I_D =30A	-	3.7	4.9	mΩ
		V_{GS} =4.5V, I_D =20A	-	5.9	9.4	
g_{FS}	Forward Transconductance	V_{DS} =5V, I_D =15A	-	28	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} =15V, V_{GS} =0V, f = 1.0MHz	-	2153	-	pF
C_{oss}	Output Capacitance		-	327	-	pF
C_{rss}	Reverse Transfer Capacitance		-	287	-	pF
Q_g	Total Gate Charge	V_{DS} =25V, I_D =30A, V_{GS} =10V	-	45	-	nC
Q_{gs}	Gate-Source Charge		-	3	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	15	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=15V, I_D=30A, R_{GEN}=3Ω, V_{GS} =10V	-	21	-	ns
t_r	Turn-on Rise Time		-	32	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	59	-	ns
t_f	Turn-off Fall Time		-	34	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	60	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	240	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_S=30A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I_F=20A,dI/dt=100A/μs	-	15	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	4	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J=25℃, V_G=10V, R_G=25Ω， L=0.5mH

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Performance Characteristics

Figure1: Output Characteristics

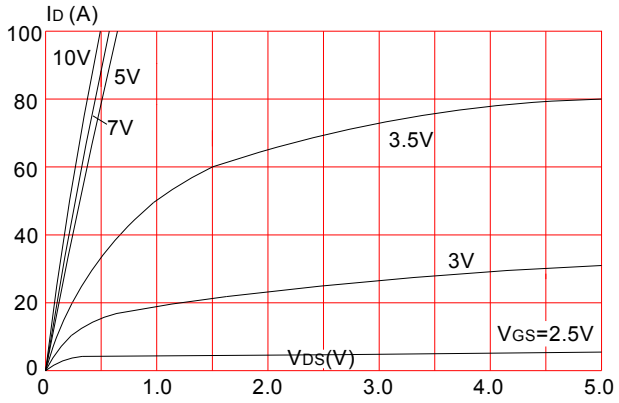


Figure 2: Typical Transfer Characteristics

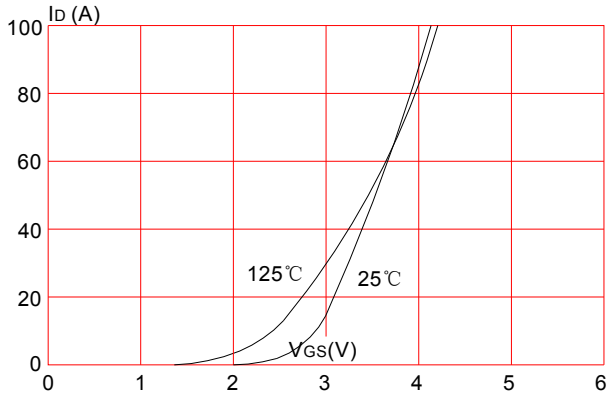


Figure 3: On-resistance vs. Drain Current

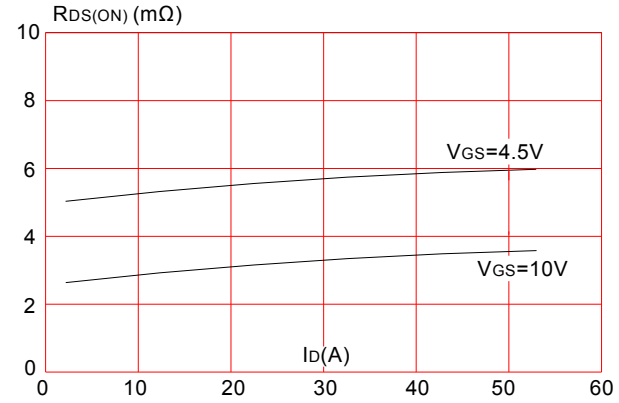


Figure 4: Body Diode Characteristics

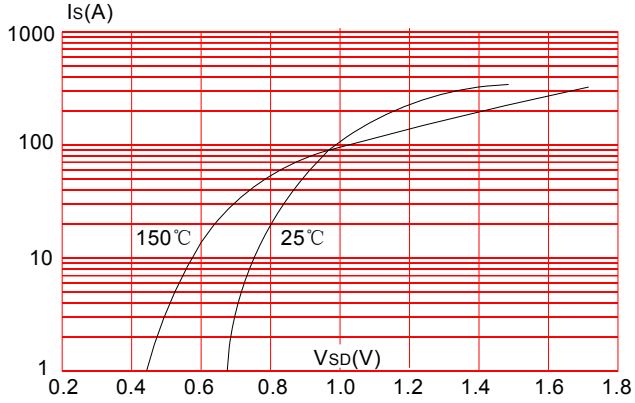


Figure 5: Gate Charge Characteristics

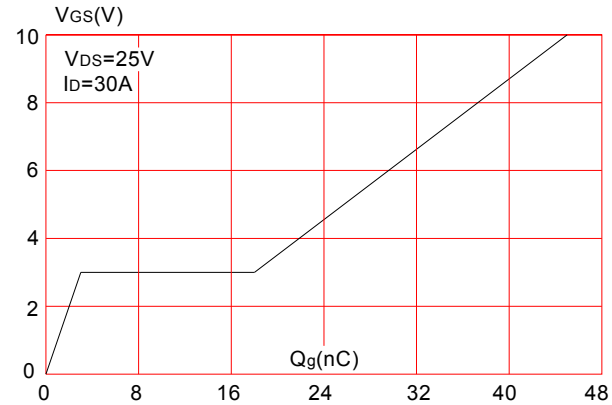


Figure 6: Capacitance Characteristics

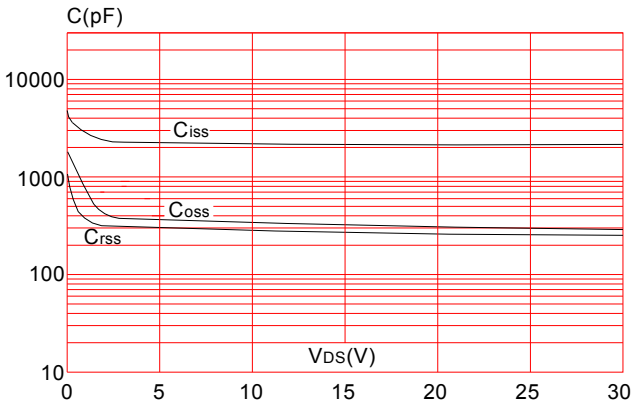


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

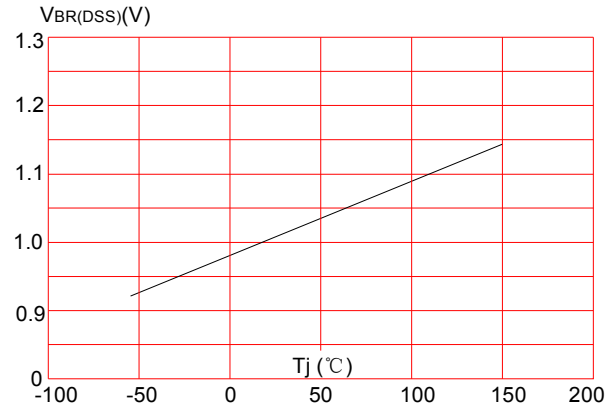


Figure 8: Normalized on Resistance vs. Junction Temperature

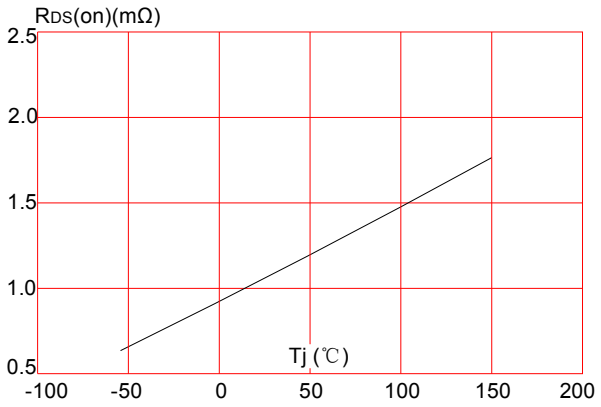


Figure 9: Maximum Safe Operating Area

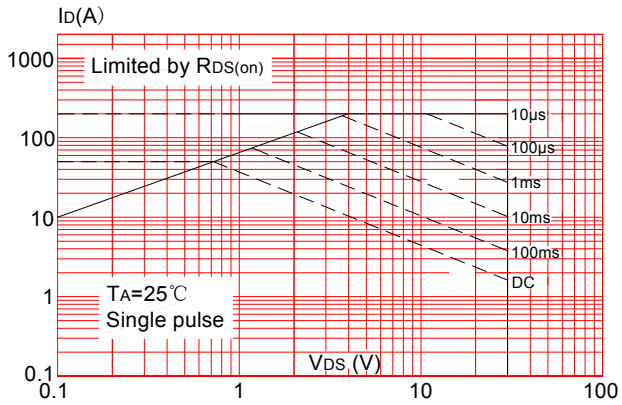


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

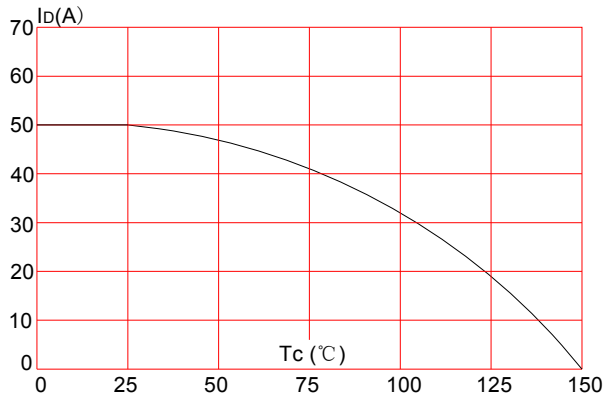
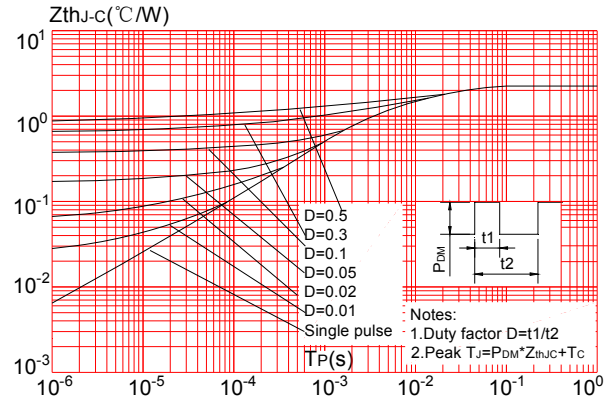


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case (PDFN5X6-8L)



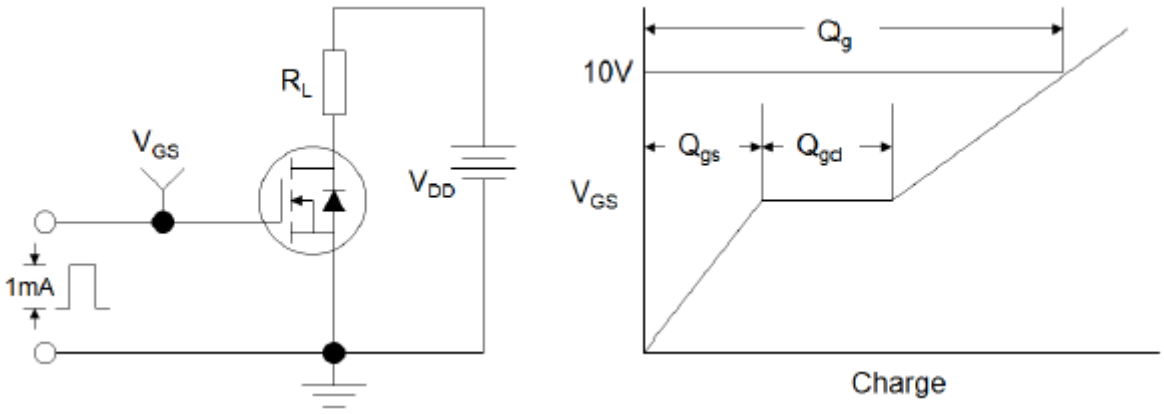


Figure1:Gate Charge Test Circuit & Waveform

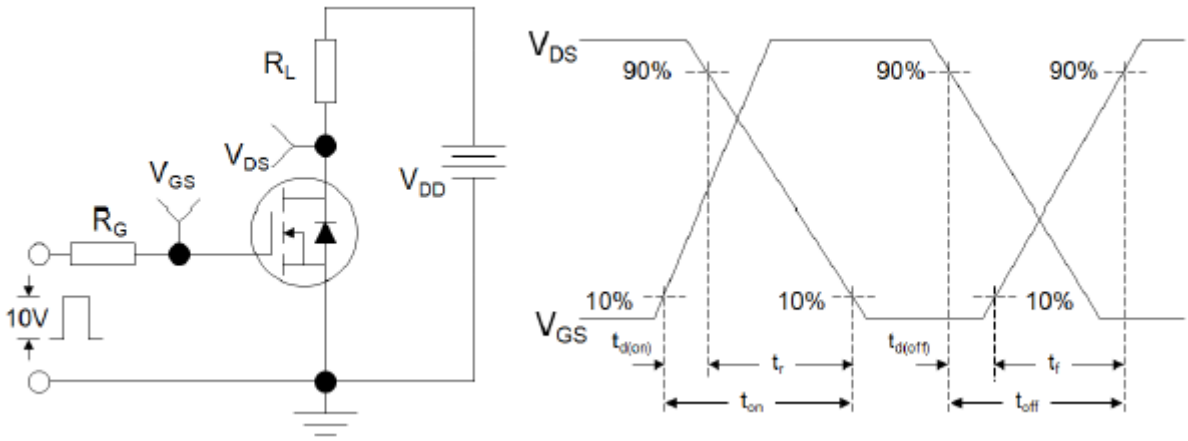


Figure 2: Resistive Switching Test Circuit & Waveforms

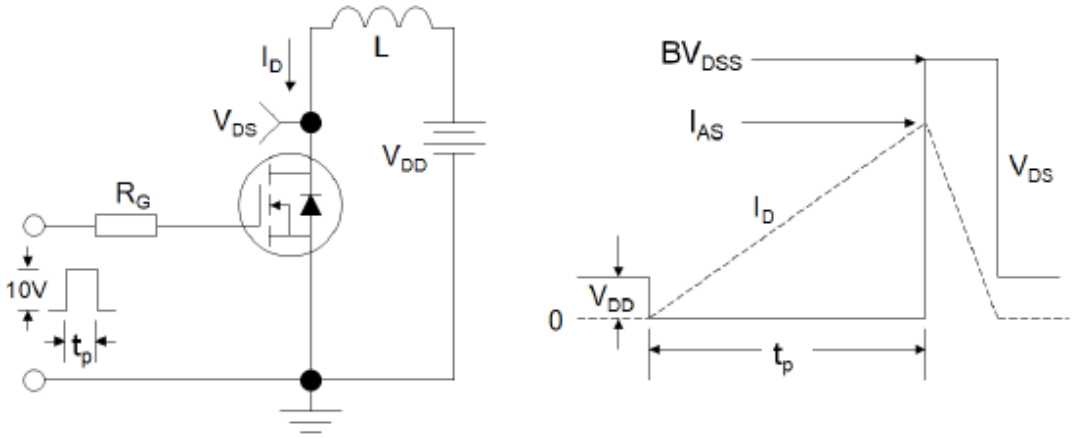


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

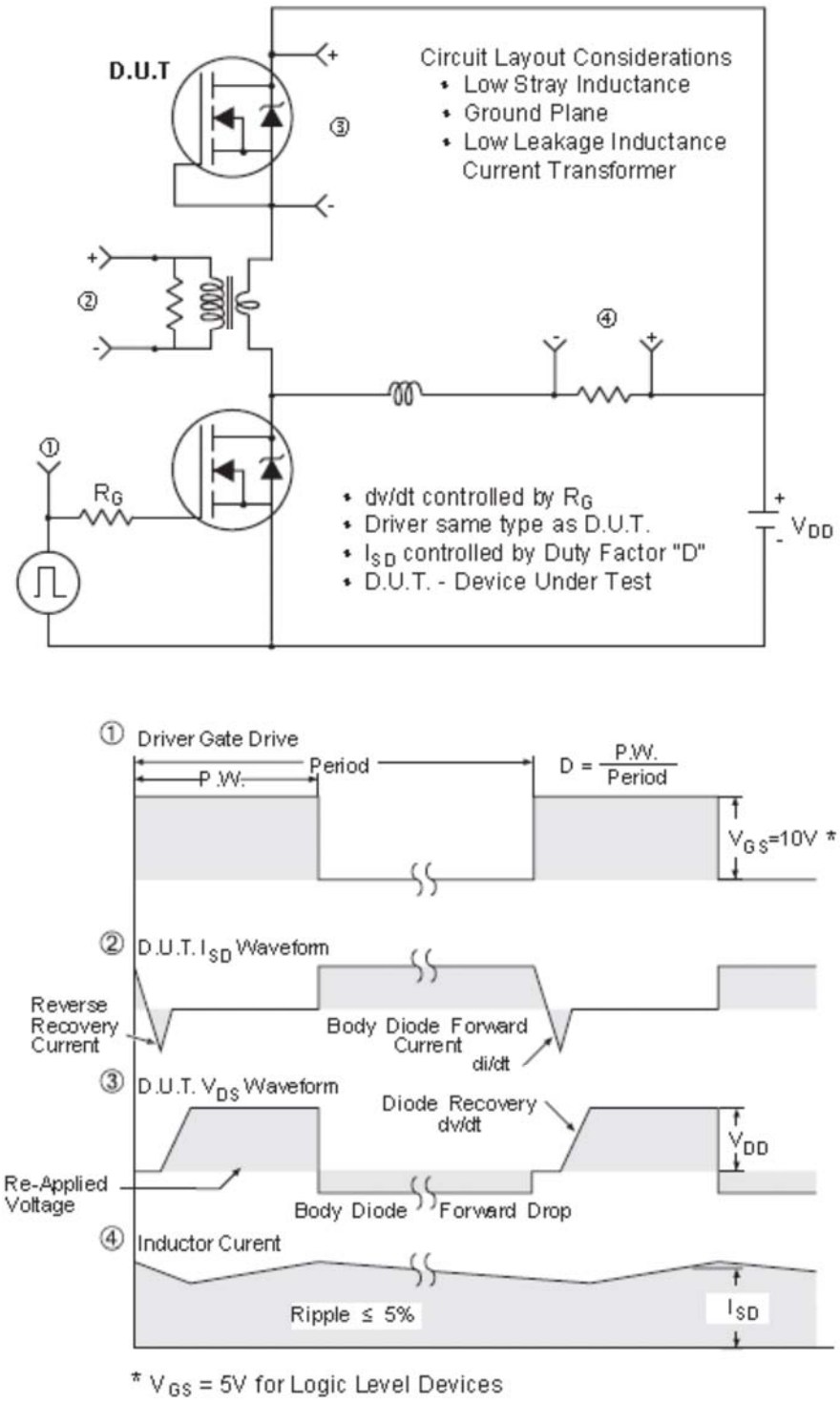
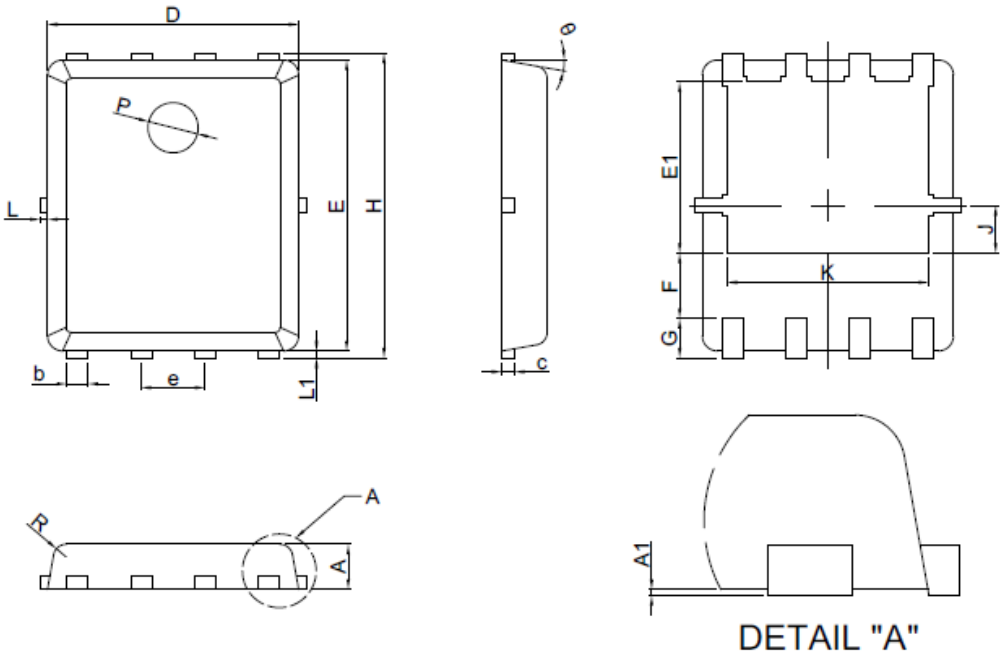


Figure 4:Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package Information : PDFN5x6-8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	0.80	1.00
A1	0.00	0.05
b	0.35	0.49
c	0.254REF	
D	4.90	5.10
F	1.40REF	
E	5.70	5.90
e	1.27BSC	
H	5.95	6.20
L1	0.10	0.18
G	0.60REF	
K	4.00REF	
L	-	0.15
J	0.95BSC	
P	1.00REF	
E1	3.40REF	
θ	6°	14°
R	0.25REF	